# The Barrel Modules of the ATLAS SemiConductor Tracker

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**Abstract**

This paper describes the silicon microstrip modules in the barrel section of the SemiConductor Tracker (SCT) of the ATLAS experiment at the CERN Large Hadron Collider (LHC). The module requirements, components and assembly techniques are given, as well as first results of the module performance on the fully-assembled barrels that make up the detector being installed in the ATLAS experiment.

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## 1. Introduction

The ATLAS experiment [1] is being constructed to explore the physics of 14 TeV proton-proton collisions at the CERN Large Hadron Collider (LHC) [2], with first beam expected in 2007. The ATLAS Inner Detector (ID) [3] tracks charged particles coming from the interaction region, and consists of a pixel detector (Pixel), surrounded by the SemiConductor Tracker (SCT), which is itself surrounded by a gaseous/polypropylene foil transition radiation tracker (TRT). The overall ID is 2.3 m in diameter and 7 m in length. For analyzing the momenta of charged particles, a 2 Tesla uniform magnetic field is provided by a superconducting central solenoid [4] which is integrated inside the cryostat of a liquid argon electromagnetic calorimeter. A quadrant view of the ID together with the solenoid is shown in Fig. 1. Because of the high energy of the proton-proton collisions, large numbers of particles are generated in one interaction, and multiple interactions are expected in one crossing of the proton bunches. The main requirements for the ID are precision tracking of charged particles in the environment of numerous tracks, capability of bunch-crossing identification, tolerance to large radiation doses, construction with the least possible material, and a capability for electron identification within the ID.

The ID consists of barrel and endcap regions in order to minimize the material traversed by particles coming from the interaction region at its centre. The barrel region is made of co-axial cylindrical layers and the endcap of disk layers. The Pixel and SCT detectors use silicon semiconductor technology for precision measurement. In the barrel region there are three Pixel and four SCT layers, each of which is able to read out a position in two dimensions. This paper describes the SCT detector modules of the barrel region. The SCT endcap modules are described elsewhere [5].

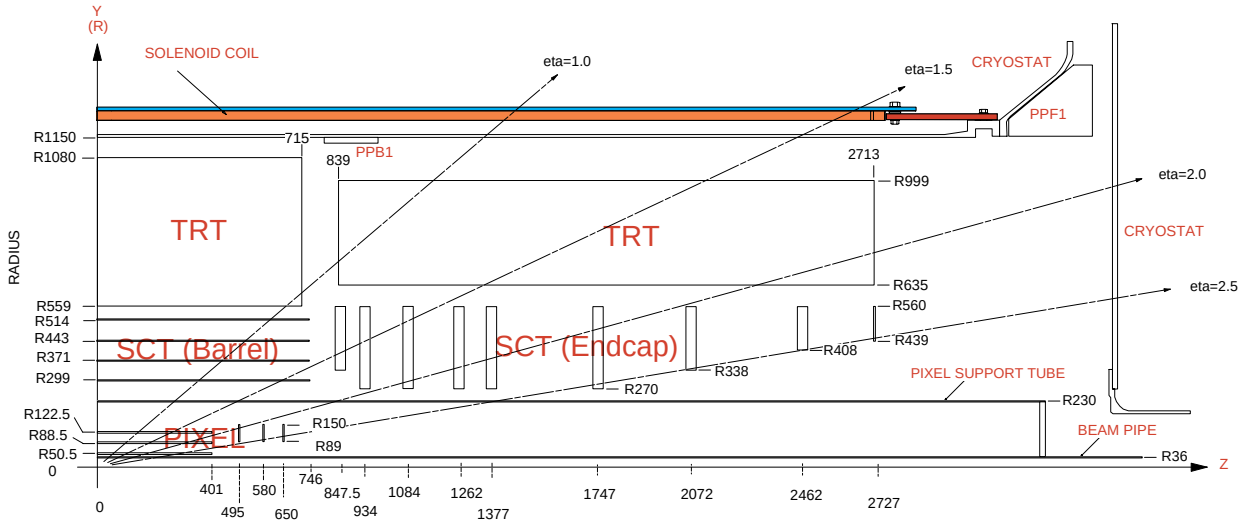



Fig. 1 A quadrant view of the inner detector (ID) together with the central solenoid inside the cryostat of the liquid argon electromagnetic calorimeter.

## 2. Design specifications

### *2.1. Overview of SCT Barrel Module Requirements*

The four SCT cylinders in the barrel region (termed Barrels 3, 4, 5 and 6) have radii between 299 mm and 514 mm and a full length of 1492 mm. Their surface areas are tiled with segmented detector elements, the SCT barrel modules, to provide complete four-layer digitization coverage for particles coming from a length of ± 76 mm about the nominal interaction point on the central axis. This is the expected ± 2 sigma length of the beam interaction point. The barrel cylinder parameters and the numbers of modules are summarized in Table 1. The design adopted for the barrel module, illustrated in Fig. 2, is to use four near-square silicon microstrip sensors, two on the top and two on the bottom side, with the readout hybrid placed near the centre of the unit. The design has minimum structure near the end edges to allow overlap of the sensitive regions of adjacent modules on a barrel. A core sheet, known as the module baseboard, provides the thermal and mechanical structure. It is sandwiched between the top and the bottom sensors, and extends sideways to include the beryllia facing regions shown in Fig. 2. The hybrid assembly bridges over the sensors and is held clear of their surfaces by feet that are glued to the beryllia facings. The module is attached to the support structure at three points, two in the large (cooling side) and one in the small (far side) facing regions. The large facing contacts a cooling element that runs along the length of the modules on a barrel.

The required tracking precision is obtained using silicon microstrip sensors with a readout pitch of 80 μm and a binary (on-off) readout scheme. The back-to-back sensor pair in a module has a stereo rotation angle of 40 mrad. A module is mounted on a barrel with its strips on one side parallel to the barrel axis (z), resulting in a precision of 17 μm in the r-phi coordinate and 580 μm in the z coordinate from the correlation obtained through fitting. The mechanical tolerance for positioning sensors within the back-to-back pair must be better than 8 μm transverse to the strip direction.

The high accumulated radiation levels at the LHC have severe consequences for silicon sensors, causing increased leakage current and type inversion, and give rise to the need to operate the sensors at about –7 $^{o}$C. The maximum expected integrated fluence after 10 years of operation in the SCT is ~$2x10^{14}$ 1 MeV-neutron-equivalent/cm$^2$ (at the upper limit of uncertainty of 50% coming from the total cross section and particle multiplicity). The corresponding sensor bias voltage required for high charge collection efficiency will be in the range 350-450 V, depending upon SCT warm-up scenarios. This will result in a total leakage current of ~ 0.5 mA for an individual sensor operated at –7 $^{o}$C at a bias voltage of 450 V. The leakage current is strongly dependent on temperature, roughly doubling every 7 $^{o}$C. The heat generation is therefore a strong function of the temperature of the sensors in the module. The power consumption of the front-end ASICs is expected to be ~5.5 W nominal and ~7.5 W maximum per module. These values are larger than originally anticipated [3], and have been amongst the driving factors in a significant evolution of the overall SCT design, and in particular that of its cooling system.

Thermal considerations, and especially the danger of thermal run-away, lead to a module design where the effective in-plane thermal conductivity must be increased beyond that of silicon. This is achieved by the use of high thermal conductivity material in the baseboard, which is laminated as part of the detector sandwich. The SCT will undergo temperature cycling over the range -20 $^{o}$C to +25 $^{o}$C in a controlled sequence, and it must survive, in the event of cooling or local power fluctuations, up to temperatures approaching 100 $^{o}$C. This requires the module to have a small coefficient of thermal expansion and to be capable of limited elastic deformation, as the precision of the tracking measurement depends on the return to a stable profile after changes in operating conditions. The SCT modules are in the tracking volume and are therefore required to have minimal mass.

Table 1: SCT barrel cylinder parameters and the number of modules

| Barrel cylinder | Radius (mm) | Length (full) (mm) | Tilt angle in phi (deg) | Number of modules |
|---|---|---|---|---|
| Barrel 3 | 299 | 1492 | 11 | 384 |
| Barrel 4 | 371 | 1492 | 11 | 480 |
| Barrel 5 | 443 | 1492 | 11.25 | 576 |
| Barrel 6 | 514 | 1492 | 11.25 | 672 |
| Total | | | | 2112 |

Note: Tilt angle is the angle of the modules relative to the local tangent to the surface of their supporting cylinder.

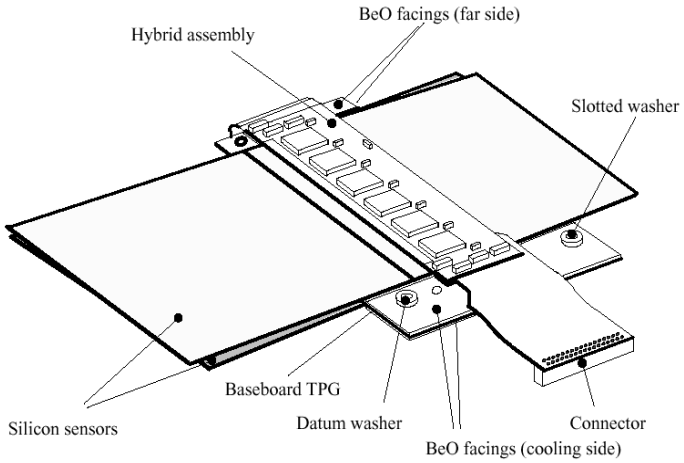



Fig. 2: A 3D-view of the ATLAS SCT barrel module. The overall length of the module is 128 mm.

### *2.2. Specifications of the components to provide the necessary module performance*

#### *2.2.1. Silicon microstrip sensors*

Full details of the SCT barrel silicon microstrip sensors are given elsewhere [6,7]. Their final specification was reached after several years of R&D. The principal requirements were to match the parameters of the chosen binary readout electronics [8] (section 2.2.3), to accommodate the high levels of radiation within ATLAS, to maximize the sensitive area of the sensor, to minimize material and to provide modules with very high tracking efficiency and low noise occupancy, both before and after irradiation. The design was also required to be simple, using single-sided processing, for economic reasons. The choice was *p*-in-*n* microstrip sensors. All 10,650 SCT barrel sensors were provided by Hamamatsu Photonics [9] and made from standard high resistivity 4-inch silicon wafers. The sensors are identical throughout the barrel SCT, with a rectangular geometry and 768 AC-coupled readout strips at a pitch of 80 μm. Table 2 summarizes their principal parameters, pre- and post-irradiation. The sensors are to be operated at about 150 V bias voltage initially. After 10 years of LHC operation, those in the innermost regions are expected to be operated at about 450 V bias voltage, with over 90% charge collection efficiency.

A corner detail of a sensor is shown in Fig. 3, where the polysilicon bias resistors, the bond pad layout and the edge bias and guard structures are visible. Some of the fiducial marks used for the mechanical alignment of sensors during module assembly (section 3.2.1) are also shown. Apart from pads used for bonding and probing, the front sides of the sensors are fully passivated. The passivation, together with stringent requirements on the quality of the cut edge (the latter being at the backplane bias voltage), are important to reduce the risk of creating accidental high voltage shorts during module construction or operation.

During pre-series production, both <111> and <100> orientations for the silicon substrate were evaluated, and found to be equally good for use in the SCT. The series production was with <111> silicon, for reasons of availability of supply. Pre-series sensors were used to make 61 (2.6%) of the SCT barrel modules. Passivation in the edge region was increased between the pre-series and main series sensor production.

Table 2: The major parameters of the SCT barrel silicon microstrip sensors

| Parameter | Value and description |
|---|---|
| Length | 63960 ± 25 μm finish (64 mm *nominal* centre cutting line to cutting line) |
| Width | 63560 ± 25 μm finish (63.6 mm *nominal* centre cutting line to cutting line) |
| Edge Quality | No edge chip or crack to extend inwards by > 50 μm |
| Thickness | 285 ± 15 μm |
| Uniformity of thickness within a sensor | 10 μm |
| Flatness | Flat when unstressed to within 200 μm |
| Wafer | *n*-type, >4 kΩ high resistivity silicon, <111> or <100> orientation |
| Implanted strips | 768 + 2 strips, *p*-implant, < 200 KΩ/cm |
| Read-out strips | 768 strips, aluminium, < 15Ω/cm, capacitively coupled with implant strips |
| Strip pitch | 80μm |
| Implant strip width | 16 μm |
| Read-out strip width | 22 μm |
| Bias resistors | Polysilicon, 1.25 ± 0.75 MΩ |
| $R_{inter\text{-}strip}$ | $>2\times R_{BIAS}$ at operating voltage after correcting for bias connection |
| Interstrip Capacitance (pre-irradiation) | Nearest neighbour on both sides, < 1.1 pF/cm at 150 V bias measured at 100 kHz |
| Interstrip Capacitance (post-irradiation) | Nearest neighbour on both sides < 1.5 pF/cm at 350 V bias, measured at 100 kHz |
| $C_{coupling}$ | ≥ 20 pF/cm, measured at 1 kHz. |
| Reach-through protection | 5 to 10 μm gap from end of implanted strip to grounded implant |
| Sensitive region to cut edge distance | 1mm |
| High Voltage Contact | Large metalised contactable *n*-layer on back. |
| Read-out pad | 200 × 56 μm bond pads, ≥ two rows, daisy-chainable |
| Passivation | Passivated on the strip side and un-passivated on the backplane |
| Identification | Every $10^{th}$ strip, starting at **1** for the first read out strip |
| Maximum operating voltage | 500 V |
| Total Leakage Current (pre-irradiation) | < 20 μA at 15 °C up to 350 V bias voltage |
| Total Leakage Current (post-irradiation) | < 250 μA at –18 °C up to 450 V bias voltage (on the sensor) |
| Microdischarge (pre-irradiation) | None below 350 V bias |
| Microdischarge (post-irradiation) | < 5% increase in the noise of any channel with bias increase from 300 V to 400 V |
| Bad strips (pre-irradiation) | A mean of ≥ 99% good readout strips per sensor, with all sensors having > 98% good strips |
| Bad strips (post-irradiation) | Number of bad strips at 350 V bias satisfying the above pre-irradiation bad strip specification |

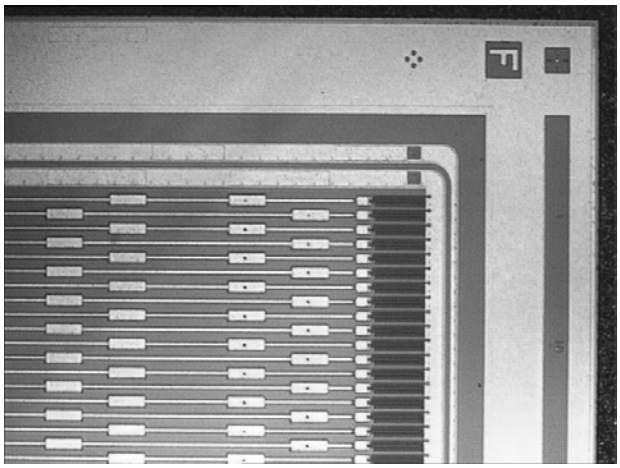


Fig. 3: Photograph of a corner of an SCT barrel silicon microstrip sensor, showing the guard structure, a selection of fiducial alignment marks, the bias ring, polysilicon resistors, and the metallization above implant strips, including wire-bonding pads.

*2.2.2. Baseboards*

The baseboard is the central element of the module, providing its thermal management, mechanical integrity and precision attachment to the barrel. Within the module the baseboard is sandwiched between the two planes of silicon sensors. To minimize the overall material within a module, the baseboard is designed to have the least possible mass compatible with both the mechanical requirements, and with providing the necessary internal heat transfer and the interface to the external heat sink. The thermal load comes from the 12 ASICs and, after irradiation, the silicon sensors (sections 2.1 and 2.3.2).

The requirements are well met by the customized thermal-mechanical baseboard shown in Fig. 4(a) and Fig. 4(b), developed specifically for this project using new processes [10]. These include directly encapsulating 380 μm thick anisotropic thermal pyrolytic graphite sheets [11] with epoxy, and at the same time interfacing 250 μm thick beryllia facing plates [12] into the structure. The highly ordered graphite crystal plane is parallel to the baseboard surface, providing the high thermal conductivity path for the heat flow, and the intrinsic fragility of such graphite plates is circumvented by the encapsulation process. The result is a baseboard with the necessary robustness, mechanical integrity and external electrical insulation, and one that is easily handled in the module construction process. The production of some 3,000 baseboards for the ATLAS SCT project was carried out at CERN by a collaboration of ATLAS members [13]. Details of the baseboard fabrication and processing are given in [14].

The larger of the two pairs of beryllia facing plates within each baseboard have holes that are aligned with similar holes in the graphite substrate to provide through-holes for attaching modules to the cylinders that support them within ATLAS. The precision alignment in the overall SCT structure comes from aluminium washers that are attached with epoxy to the upper beryllia facing plate of the baseboard. The washers are positioned above the through-holes using jigs that set the relative separation of their centres and also the orientation of their line of centres [14]. One washer has a circular hole of diameter 1.800 mm, tolerance (−0.005, + 0.010) mm, which determines a precise spatial location for the module, and the second washer maintains similar precision in the direction perpendicular to the module sensor strips while its opening is slotted in the other direction to provide for mechanical tolerances in assembly. These washers can be seen in Fig. 4(a). Module attachment to the cylinder within ATLAS is completed through a clamped third mounting point at the edge of the small beryllia facing.

Electrical high voltage bias contact to the back surface of the attached silicon wafers is through areas where the encapsulation is removed from the baseboard surfaces during production, and electrically conducting epoxy is applied during the wafer attachment process (section 3.2.1). The bias connectivity is completed using the electrical conductivity of the graphite core, via small holes, filled with electrically conducting epoxy [14], in the small and large facings within the upper surface of the baseboard (see Fig. 4(a)). The holes in the beryllia facings have gold-plated surround pads that subsequently allow connection to be made with wire-bonds to the bias potential supplied from the module hybrid (section 3.2.4). These features can be seen in the picture of the upper side of a baseboard in Fig. 4(a), while beryllia facings without bias contacts or washers are shown on the lower-side of the baseboard in Fig. 4(b), and are inclined by 40 mrad with respect to those on the upper surface for purposes of silicon sensor mounting (section 2.3.1).

When assembled in the SCT, the conducted heat leaves the module via the larger beryllia facing on the baseboard lower surface, which is interfaced to an aluminium block via a layer of thermal grease, approximately 100 μm thick, and a copper-kapton shunt-shield. The block itself is soldered to a cooling pipe in which the heat is used as latent heat to evaporate liquid $C_3F_8$ at temperatures close to −25 $^0$C.

The baseboard properties are summarized in Table 3.

Table 3: Specifications of the SCT barrel baseboard

| Parameters | | Central Value | Tolerance Limit |
|---|---|---|---|
| Thermal pyrolytic graphite substrate: | | | |
| (i) | in-plane thermal conductivity | 1650 W/m K at 20 °C | >1450 W/m K at 20 °C |
| (ii) | transverse thermal conductivity | ~6 W/m K | |
| Encapsulated baseboard thickness in sensor area | | 430 μm | ± 50 μm |
| Baseboard thickness in beryllia facing area | | 930 μm | ± 70 μm |
| Beryllia facing thermal conductivity | | ~280 W/m K at 20°C | |

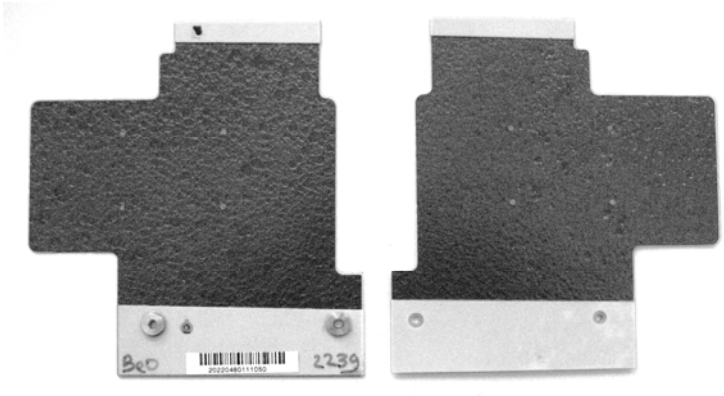


Fig. 4: (a) Baseboard Upper surface (b) Baseboard Lower Surface

*2.2.3. ASICs*

The ABCD3TA chip provides all functions required for processing the signals from 128 strips of a silicon strip detector in the ATLAS experiment. It is a single chip implementation of a binary readout, using DMILL technology. The main functional blocks are front-end, input register, pipeline, de-randomizing buffer, command decoder, readout logic, and threshold and calibration control sections. The die size of the ABCD3TA chip is 6550 μm x 8400 μm. The full details of the ASIC are described elsewhere [8].

The main requirements of the chip are summarized in Table 4 and the pad layout is shown in Fig. 5. The front-end section performs charge integration, pulse shaping and amplitude discrimination. The threshold value for the amplitude discrimination is provided as a differential voltage from an internal programmable DAC. The outputs of the discriminators are latched either in the edge-sensing mode or in the level-sensing mode. At the start of each clock cycle the chip samples the outputs from the discriminators and stores these values in a pipeline until a decision can be made on whether to keep the data. Upon receipt of a Level 1 Trigger signal the corresponding set of values, together with their neighbours in time, are copied into the readout buffer serving as a de-randomizing buffer. The data written into the readout buffer are compressed before being transmitted off the chip. Transmission of data from the chip is by means of token passing. The chip incorporates features that, with the hybrid circuit, enable the system to continue operating in the event of a single chip failure. It is a system requirement that less than 1% of data will be lost due to the readout buffer on the chip being full, provided that the average occupancy of the silicon strip detectors is below 2% at an average trigger rate of 100 kHz. This is to be compared with the expected worst case strip occupancy averaged over strips and time, which is only 1%.

The ABCD3TA design provides uniformity of thresholds, a critical parameter for the binary architecture, by implementation of an individual threshold correction in every channel using a 4-bit digital-to-analogue converter (TrimDAC) per channel. The TrimDAC has four selectable ranges to cope with the spread of threshold offsets, which increases by a factor of three after a fluence of $3 \times 10^{14}$ protons/cm$^2$.

Each channel has an internal Calibration Capacitor connected to its input for purposes of simulating a hit strip. The Calibration Capacitors are charged by an internal chopper circuit that is triggered by a command. Every fourth channel can be tested simultaneously, with group selection determined by two binary coded Calibration Address inputs. The voltage step applied to the Calibration Capacitors by the chopper is determined by an internal DAC. A tuneable delay of the calibration strobe with respect to the clock phase covers approximately two clock periods.

Table 4: Requirements of the ABCD3TA chip

| Parameter | Description |
|---|---|
| Signal polarity | Positive signals from *p*-type strips |
| Input protection | voltage step of 450 V of either polarity with a cumulative charge of 5 nC in 25 ns |
| Gain at the discriminator input | 50 mV/fC |
| Peaking time | 20 ns |
| Noise (ENC) on fully populated modules | Typically 1500 electrons rms for an unirradiated module |
| | Typically 1800 electrons rms for an irradiated module |
| Noise occupancy at 1fC threshold | $< 5x10^{-4}$ |
| Threshold setting range | 0 fC to 12.8 fC with 0.05 fC step |
| Timewalk | 16 ns (1.25 fC to 10 fC with 1fC threshold) |
| Double Pulse Resolution | 50 ns for a 3.5 fC signal followed by a 3.5 fC signal |
| Power consumption (of fully populated module) | < 6 W nominal |

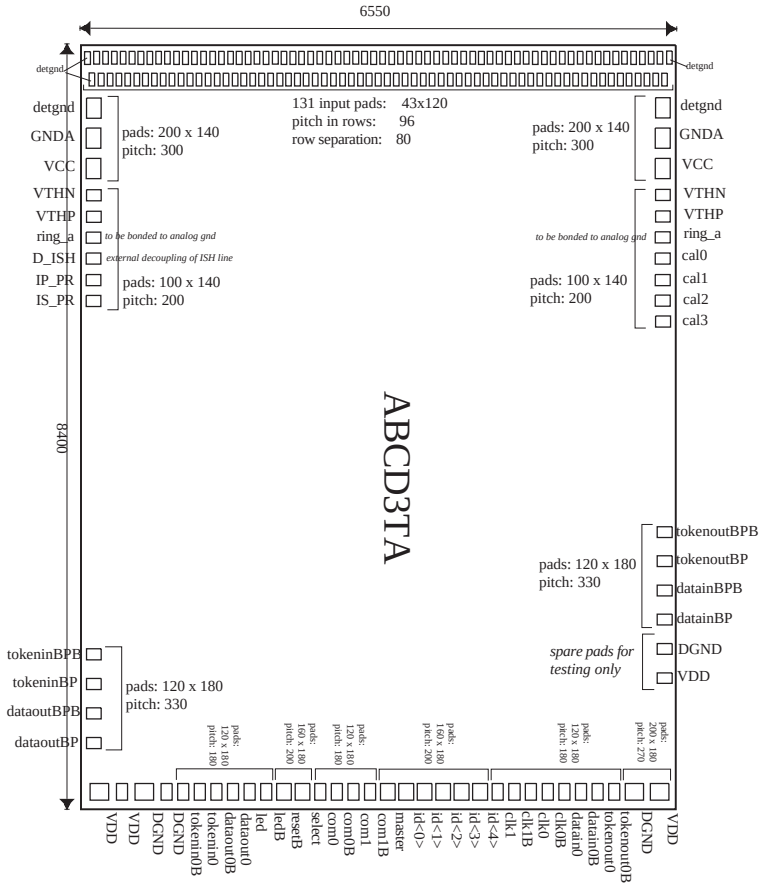



Fig. 5: The pad layout of the ABCD3TA chip.

### *2.2.4. Hybrids*

The SCT barrel hybrid carries electrical circuitry and 12 ABCD3TA readout chips, 6 on the top side (termed link0) and 6 on the bottom side (link1). It is also required to have mechanical rigidity, a high thermal conductivity for transferring generated heat from the ASICs, and a small fraction of a radiation length of material. Since the hybrid is bridged over the sensors, with a gap in between, the bridge material must be rigid enough to make ultrasonic wedge bonding of aluminium wire possible.

The design uses a Cu/Polyimide flexible circuit for the electrical functions and a carbon-carbon substrate for the mechanical and thermal functions. The Cu/Polyimide flexible circuit technology has been widely used in

industry. The use of laser vias and build-up layers allows the hybrid to be both small and thin. A benefit of using a flexible circuit is that it enables the hybrid and cable sections to be made as a continuous piece so that vulnerable connections between the two are eliminated. The technology used in this hybrid is described in detail elsewhere [15].

The dimensions of the SCT barrel hybrid are displayed in Fig. 6. The electrical schematics are shown in Fig. 7 and Fig. 8, where Fig. 7 is for the 6 chips on the top side of the module, link0, and Fig. 8 for the 6 chips on the bottom side of the module, link1. Each link has one master chip, which is responsible for the transmission of data off the module. The last chip of a link is set to an end function, and the rest of the chips are set to a slave function. The data and tokens are passed between the adjacent chips with "datain0/dataout0" and "tokenout0/tokenin0" pads at the back-end of the chips (Fig. 5). In the case of a failure, a chip is skipped by using the "datain1/dataout1" and "tokenout1/tokenin1" pad connections at its side. The digital and analogue ground connections are made on the hybrid, at the side of every ASIC.

The hybrid is made of four copper layers, whose functions are summarized in Table 5. The middle two layers, L2 and L3, extend through the flexible circuit from the connector to the far-end of the hybrid, and L3 is continuous to make the resistivity of the grounds as small as possible. The thickness of the copper is 12 μm. The ground and power planes of layers L1 and L4 are meshed with 50% openings to compensate for an increase in material from the metallization of through-holes and vias causing thickening to 30 μm. The thickness of the flexible circuit at the hybrid section is 280 μm.

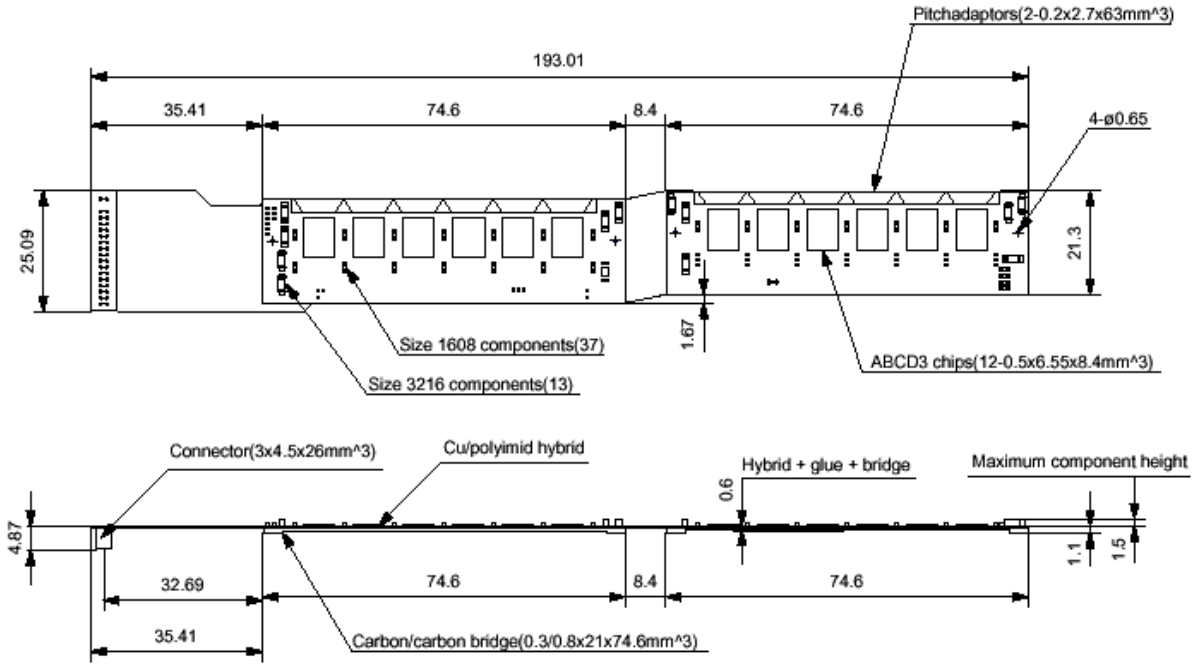



Fig. 6: Dimensions (in mm) of the SCT barrel hybrid

Table 5: Function of each of the four Cu layers of the SCT barrel hybrid

| Layer (from top) | Function |
|---|---|
| L1 | Pads for wire-bonding, traces to the pads from the bus lines along the hybrid in L2 |
| L2 | Bus lines along the hybrid, power supply planes in the cable section |
| L3 | Analogue and digital ground planes continuous from the connector to the far-end of the hybrid |
| L4 | Power supply planes for the analogue and the digital sections |

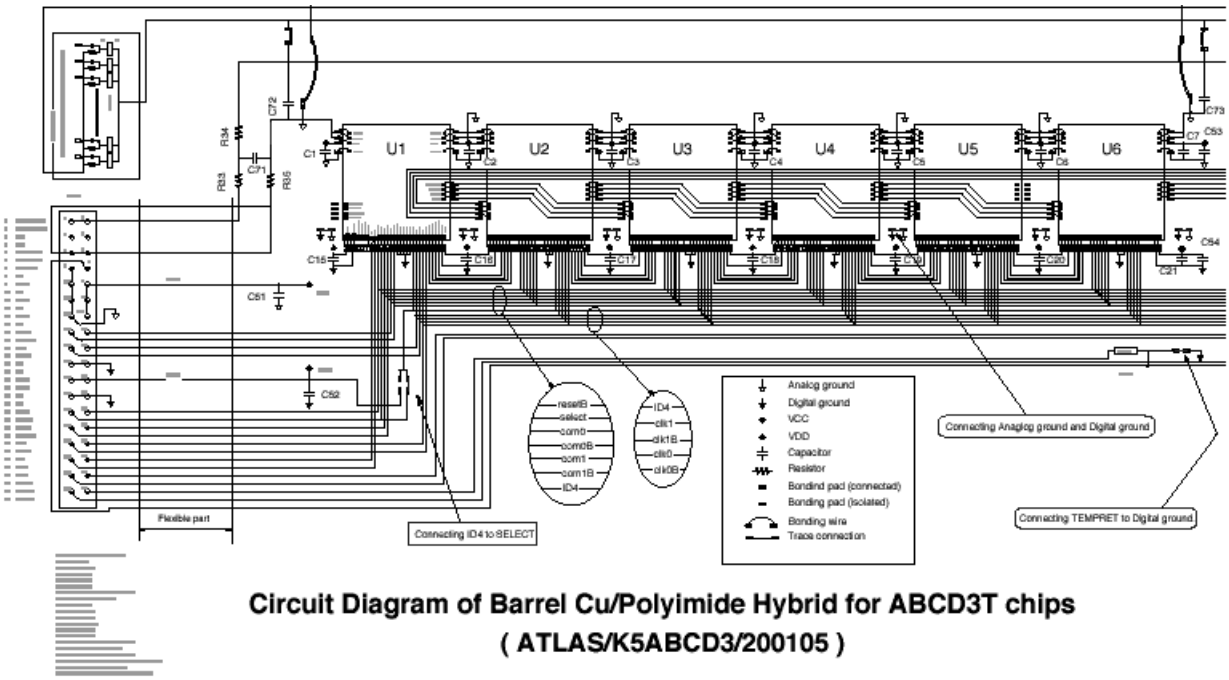



Fig. 7: Circuit diagram of SCT barrel hybrid (connector and link0 circuitry)

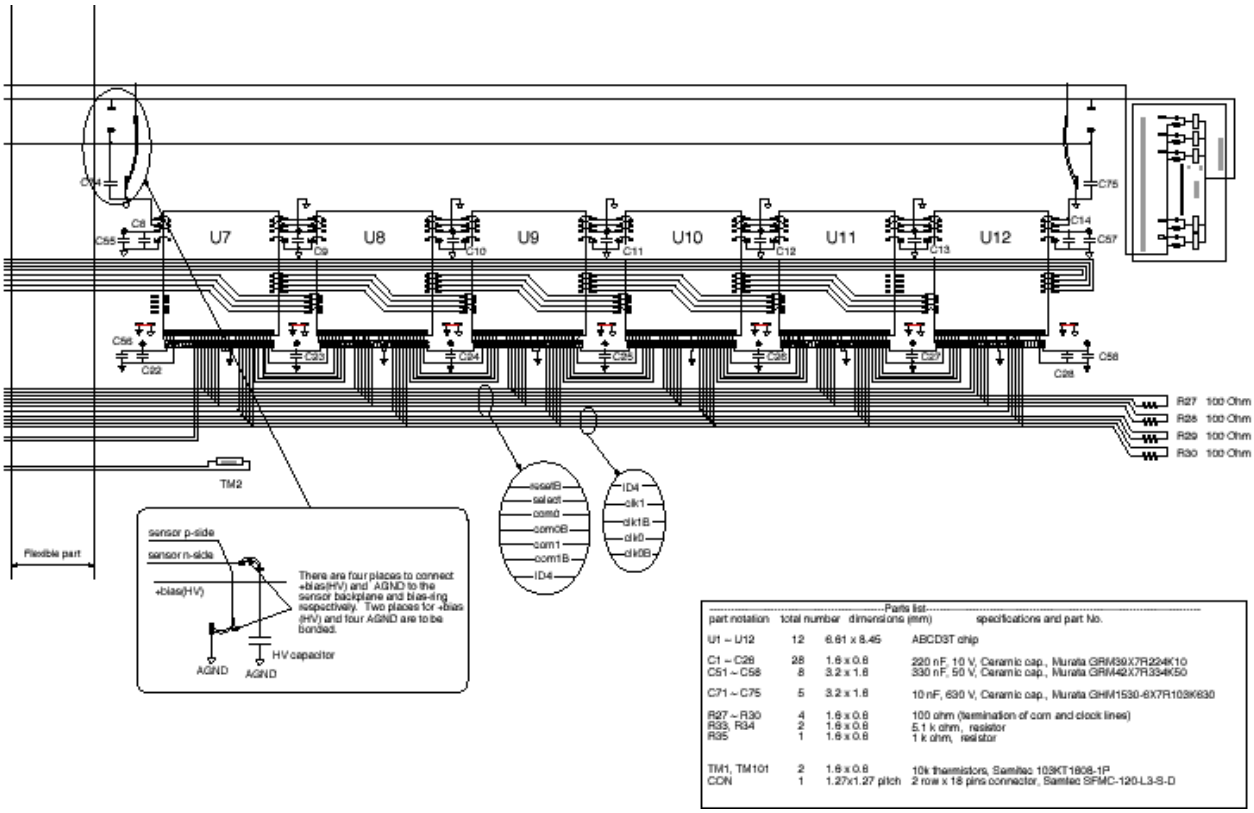



Fig. 8: Circuit diagram of the SCT barrel hybrid (link1)

The Cu/Polyimide flexible circuit is reinforced with a bridge to provide good thermal conductivity and high Young's modulus, with only a small fraction of a radiation length of material. The bridge substrate is made of carbon-carbon material with uni-directional fibres along the length of the hybrid to maximize the thermal conductivity. It is connected electrically to the ground of the hybrid and ASICs. The properties of carbon-carbon are summarized in Table 6 and the specification of the bridge is shown in Fig. 9. The surface of the bridge is coated with a polymer, Parylene, to a thickness of 10 μm, to provide insulation and improve reliability for handling. The surface of this coating is roughened with a laser where adhesion is required, and the coating is removed where electrical and thermal conduction are necessary.

The pitch of the input pads of the ASIC is 48 μm, whereas that of the silicon microstrip sensors is 80 μm. In order to make simple parallel wire-bonding, a pitch-adapter is used in front of the ASICs. Because of the fine pitch, the pads and traces are fabricated on a glass substrate with a thin aluminium deposition. The size of the pitch adapter is 63 mm (long) x 2.7 mm (wide) x 0.2 mm (thick). The thickness of aluminium is in the range 0.9 μm to 1.0 μm. The fabrication details for the pitch-adapter are described in [15].

In order to transfer the heat from the ASICs and to connect their ground to the carbon-carbon bridge, a set of 17 through-holes per chip is placed in the hybrid ASIC analogue section. The through-holes are 300 μm in diameter, plated with Cu of 20 μm thickness, and filled with silver-loaded electrically conductive adhesive. The effective thermal conductivity of these "pillars" is estimated to be about 40 W/m K.

Two thermistors, one per link, are equipped to monitor the temperature of the hybrid. The temperature is readily calculated from the measured resistance, $R$, as

$$R = R25 \exp(B(-1/T+1/T25)) \quad (1)$$

where the temperature, $T$, is given in Kelvin and $R25$ and $T25$ are the nominal resistance and the temperature (in Kelvin) at 25 $^{o}$C, respectively. The thermistors have $R25$ = 10 kΩ ± 1% and $B$ = 3435 K ± 1%.

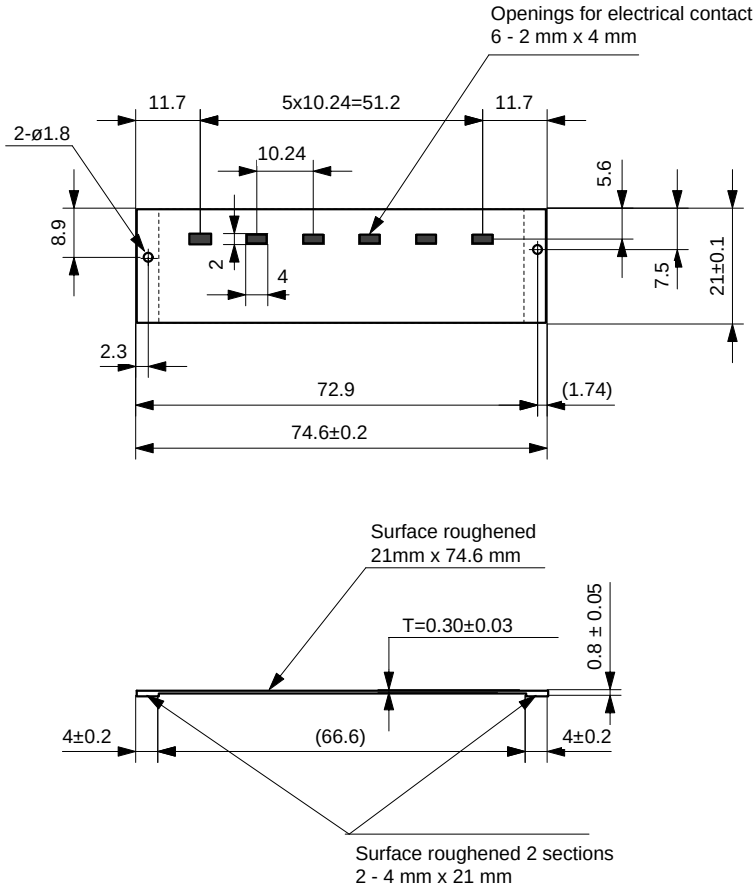



Fig. 9: Specification of the hybrid carbon-carbon bridge (dimensions in mm).

Table 6: Properties of the hybrid carbon-carbon substrate material

| Parameter | Description |
|---|---|
| Carbon fibre direction | Uni-directional |
| Thermal conductivity (fibre direction) [W/m K] | 700 ± 20 |
| Thermal conductivity (transverse to fibres) [W/m K] | 35 ± 5 |
| Young's modulus (fibre direction) [GPa] | 294 |
| Thermal expansion coefficient (CTE) (fibre direction) [ppm/K] | −0.8 |
| Thermal expansion coefficient (CTE) (transverse to fibres) [ppm/K] | 10 |
| Electrical resistivity (fibre direction) [Ωm] | $2.5 \times 10^{-6}$ |
| Density [$g/cm^3$] | 1.9 |
| Percentage of radiation length [%Xo] | 0.26 |

### *2.2.5 Adhesives*

The barrel modules are constructed from the four major components described above; the silicon microstrip sensors, baseboards, ASICs and hybrids. They are joined together with thermally conductive and electrically conductive epoxy adhesives. Epoxy adhesives are chosen since they are known to be radiation-tolerant up to a very high fluence.

A thermally conductive adhesive is required in order to transfer the heat generated in the sensors into the baseboard. This is critical, especially after accumulating a large fluence of particles which damage the silicon bulk and induce an increase of many orders of magnitude in the leakage current, together with increased full depletion voltage. The sensors may run away thermally through positive feedback of the leakage current and the temperature unless the heat from the sensors is transferred to the baseboard efficiently. Thermally conductive epoxy is also used for other joints where thermal conduction is required, such as the attachment of the hybrid to the beryllia facings of the baseboard (section 2.2.2).

An electrically conductive epoxy is required because the baseboard, made of carbon, is used for the electrical conductive path from the bias line on the hybrid to the backplane of the sensors. The readout ASICs are also attached to the hybrids with electrically conductive epoxy.

The thermally conductive epoxy used is a two part, room temperature curing epoxy, known as Araldite 2011 [16]. In order to enhance its thermal conductivity, a boron-nitride (BN) filler is added [17]. Boron-nitride was chosen in preference to alumina for this filler as tests with alumina showed that some increase was caused in the leakage current of the glued sensors. The resin, hardener and filler are mixed by weight in the proportions 38.5%, 30.75% and 30.75%, respectively. The thermal conductivity of the mixture is estimated to be about 1 W/m K.

The electrically conductive epoxy used is a two part, low temperature curing epoxy, Eotite p-102 [18]. Although the listed curing temperature is above 50 $^{o}$C for this product, the epoxy will cure at room temperature after sufficient time (for example, 24 h at 23 $^{o}$C).

## *2.3. Specifications for the assembled module*

### *2.3.1. Mechanical specification*

Each barrel module contains four 63.96 mm x 63.56 mm (cut-edge to cut-edge) single-sided silicon microstrip sensors. The geometrical alignment of the two sensors on one side, to form a 128 mm long unit, is shown in Fig. 10. The strips of the two sensors are wire-bonded to form 126 mm long strips in a later stage of the assembly (section 3.2.4). The pitch of the strips is 80 μm and there are physically 770 strips, with the first and the last being connected to the strip bias potential for electric field shaping and for defining the strip boundary. The sensors have been designed to have a minimum guarding region around their edges, consistent with their high voltage performance requirements. The distance between the sensor cut edge and sensitive region is 1 mm (section 2.2.1), which results in a dead region of ~2 mm length in the centre of the module.

Some principal barrel module parameters are summarized in Table 7. The sensors and hybrid on the two sides are rotated around the "module physics centre", by ± 20 mrad. The "module physics centre" is the geometrical centre of the four sensors. The support structure of the module on the barrel cylinder rotates the module around the "module physics centre" by a further ± 20 mrad so that strips on one side of the module are parallel to the axis of the barrel cylinder and those on the other side are at ± 40 mrad to the axis, the sign alternating for successive barrels.

The nominal thicknesses of the module are: 1.15 mm in the sensor area, 0.93 mm in the beryllia facing area, 3.28 mm in the blank hybrid area, 6.28 mm in the highest hybrid component area, 4.48 mm in the ASIC area, and 5.08 mm in the highest wire-bond area. Since wire-bonds have height variations, at least a 1 mm stay-clear distance is required in elevation, and so the module stay-clear thickness in the highest wire-bond area is 7.08 mm. The wrap-around part of the hybrid interconnect cable extends to a distance of between 40.0 mm and 41.22 mm from the module centre, depending on the shape at the wrap-around.

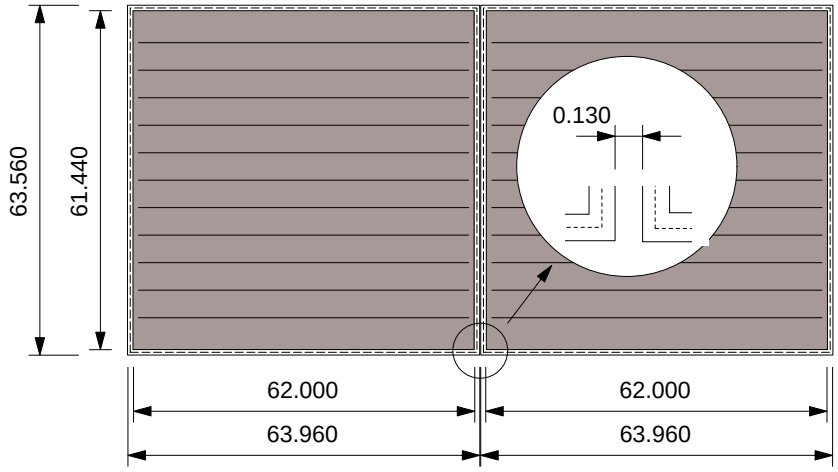



Fig. 10: Geometrical alignment of the two silicon microstrip sensors in the SCT barrel module. The shading represents their sensitive area. Units are in mm.

Table 7: Some SCT barrel module mechanical, electrical and thermal specifications

| Parameter | Description |
|---|---|
| Silicon outer dimension | 63.56 mm x 128.05 mm (cut-edge) |
| Construction | Four 63.56 mm x 63.96 mm *p*-in-*n* single-sided sensors to form back-to-back glued sensors |
| Mechanical alignment tolerance | back-to-back: < 8 μm (in-plane lateral, X), < 20 μm (in-plane longitudinal, Y), < 70 μm (out-of-plane, Z, deviation from the average profile) |
| | Fixing point: < 40 μm (X), < 40 μm (Y) |
| Strip length | 126.09 mm (2.090 mm dead in the middle) |
| Strip directions | ±20 mrad (0, ±40 mrad on support structure) |
| Number of readout strips | 768 per side, 1536 total |
| Strip pitch | 80 μm |
| Hybrid | one-piece hybrid wrapped around the module |
| Hybrid power consumption | 5.5 W nominal, 7.5 W maximum |
| Maximum sensor bias voltage | 460 V (on the detector), up to 500 V in the module |
| Operating temperature of sensor | −7 °C (average) |
| Uniformity of silicon temperature | < 5 °C |
| Maximum irradiated sensor power consumption | 1 W total at −7 °C, Heat flux (285 μm): 120 μW/mm$^2$ at 0°C |

There is a maximum error of about 500 μm in the connector position on the hybrid 'pigtail' cable (Fig. 2), coming from both the error in the connector placement within the hybrid and that of the hybrid placement in the module. The flexible pigtail cable has to connect to a less flexible opto-harness on the barrel cylinder [19]. The hybrid pigtail cable is sufficiently long to allow its route to be adjusted to achieve the correct mating between the two connectors.

The cut edge of the sensor is conductive and at the high voltage of the backside of the sensors. Thus conducting debris between the cut edge and ground could cause high voltage shorts. A stay-clear distance of at least 1 mm is imposed between the sensor edge and any other ground potential when the module is mounted on the barrel, which assures a high voltage breakdown of 3 kV to ground at sea level in air [20]. The centres of adjacent modules are separated by 2.8 mm in height on the cylinders. This distance leaves a nominal stay-clear distance of 1.65 mm between a cut edge and the opposing sensor surface, after allowing for 400 μm in thickness tolerances and 200 μm in non-planarity tolerance of overlapping modules.

The layout of modules mounted on a barrel is illustrated in Fig. 11. The visible features include the overlap of the silicon of neighbouring modules, the stereo angle of the lower silicon sensors within a module and the hybrid pigtail connection.

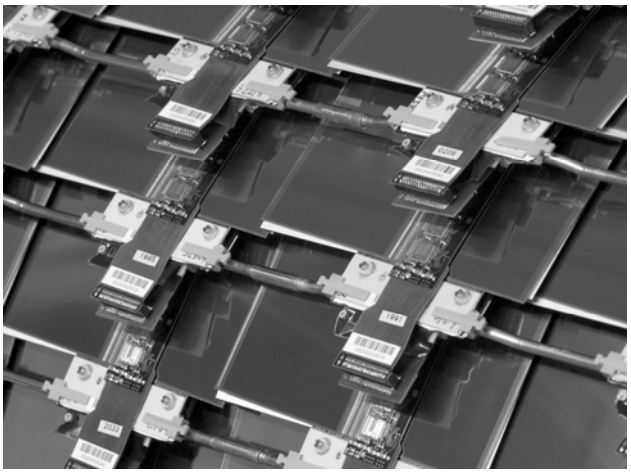


Fig. 11: A photograph of modules mounted on a barrel cylinder. The large beryllia facings of the modules are connected mechanically by PEEK clips and thermally by grease to heat sinks, which are aluminium blocks with copper-kapton shunt-shields, soldered to the visible Cu/Ni cooling pipes (which have 70 μm wall thickness).

### *2.3.2. Thermal Specification*

The module design must be safe against thermal runaway of the silicon sensors throughout the lifetime of the SCT. The requirement is also to maintain the sensors at a uniform temperature of about –7 $^0$C to reduce the reverse annealing of the silicon and the bulk leakage current after radiation damage (section 2.1). The module design was therefore developed with the help of thermal Finite Element Analysis (FEA) simulations. The bulk heat generation after 10 years of operation at LHC is estimated to be 120 μW/mm$^2$ at 0 $^o$C in the silicon microstrip sensors in the worst case (Table 7). The calculated thermal profile of the module is shown in Fig. 12 for a hybrid power consumption of 6.0 W and a heat sink temperature of –14 $^o$C at the cooling contact (which is the large beryllia facing that contacts the cooling block on a barrel, Fig. 11, through thermal grease and a copper-kapton shunt-shield). The highest temperature of the module is at the ASIC in the middle of the hybrid, and is about 20 $^o$C above the heat sink temperature. The maximum ($T_{si}$ max) temperature of the silicon sensors is about 10 $^o$C above the heat sink temperature, at the top left corner of the sensor. The $T_{si}$ max temperature as a function of the bulk heat generation, normalized at 0 $^o$C, is shown in Fig. 13 for a hybrid power consumption of 6.0 W and heat sink temperatures of –14 $^0$C and –17 $^o$C. The simulation shows that thermal runaway of the silicon sensor would occur at 280 μW/mm$^2$ at −14 $^o$C heat sink temperature, which gives a safety factor of 2.3 against thermal runaway for the estimated final heat generation of 120 μW/mm$^2$. For a hybrid power consumption of 8 W, in excess of the anticipated maximum of ~ 7.5 W, a slightly lower heat sink temperature of –17 $^o$C is required to give a similar safety factor, with thermal runaway at 290 μW/mm$^2$. A temperature of –17 $^o$C at the module cooling interface can be achieved by operating the SCT evaporative cooling system at –25 $^o$C, which is within its design specification.

### *2.3.3. Mass specification*

The module has to be designed to minimize the material presented to particles. The target figure within the initial overall ATLAS detector design was 1.2% of a radiation length, averaged over the module area, for particles at normal incidence to the silicon [3]. The calculated radiation length fractions and masses of the components for the final module design are summarized in Table 8. The actual weights of components have been measured and the results match the estimated values to within a few percent. The maximum contribution comes from the silicon sensors, and their thickness was reduced from a standard 300 μm to 285 μm (section 2.2.1) to reduce the material budget (and also the full depletion voltage). The overall mass of the module is 25 g and the percentage radiation length averaged over the silicon sensor area is 1.17% $X_o$. This therefore matches the ATLAS requirement for the module. The total material in the as-built SCT barrel detector averages ~3% $X_o$ per layer, and is dominated by the module services.

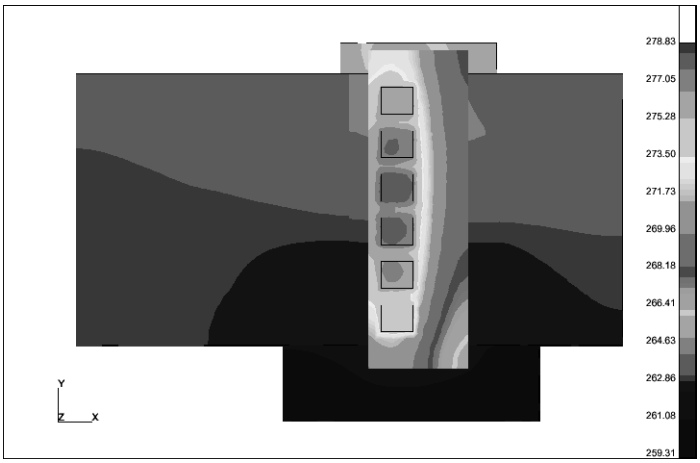



Fig. 12: An FEA simulation of the thermal profile of the SCT barrel module, with the maximum heat generation in the silicon microstrip sensors, 120 μW/mm$^2$, a hybrid power consumption of 6 W, and a heat sink temperature of –14 $^0$C at the cooling contact. The highest and the lowest temperatures are +5.7 $^0$C and –13.8 $^0$C, respectively.

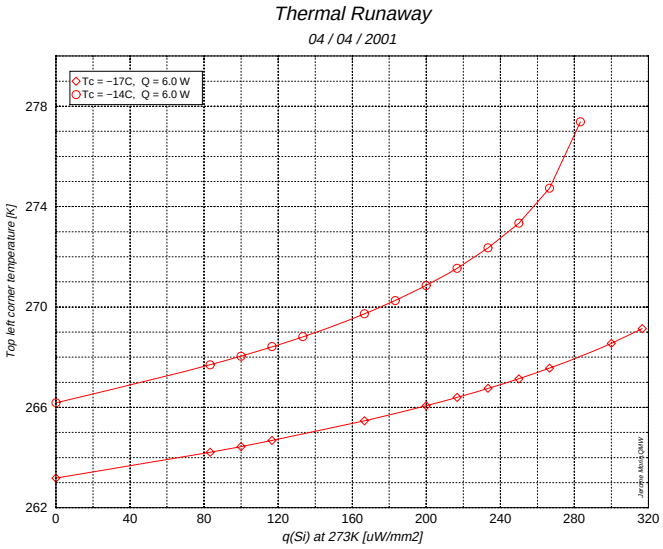



Fig. 13: Temperature of the hottest point in the sensors as a function of heat generation for a hybrid power of 6 W, with the heat sink temperatures of –14 $^0$C (upper curve) and –17 $^0$C (lower curve).

Table 8: Radiation length percentages and masses estimated for the SCT barrel module

| Component | Percentage of a radiation length [%Xo] | Mass [g] | Fraction of total module mass [%] |
|---|---|---|---|
| Silicon sensors and adhesives | 0.612 | 10.9 | 44 |
| Baseboard and BeO facings | 0.194 | 6.7 | 27 |
| ASICs and adhesives | 0.063 | 1.0 | 4 |
| Cu/Polyimide/CC hybrid | 0.221 | 4.7 | 19 |
| Surface mount components | 0.076 | 1.6 | 6 |
| Total | 1.17 | 24.9 | 100 |

### *2.3.4. Electrical performance*

The criteria for the module to be classified as electrically good are shown in Table 9. The strip 'micro-discharge' criterion relates to the fact that the anticipated radiation levels during ATLAS running are a factor of two larger for Barrel 3 than for Barrel 6. After 10 years of ATLAS operation (with the LHC as presently approved) and the corresponding radiation damage and type inversion of the silicon sensors, it is expected that the modules on Barrel 3 will need to be operated at ~ 450 V bias for ~90% charge collection efficiency, while those on Barrel 6 will operate at ~ 250 V bias. The initial operation within ATLAS is expected to be at 150 V bias for all barrels. The electric field configuration and high voltage properties of sensors are different after type inversion following irradiation. All SCT sensors are specified to operate up to 500 V post-irradiation (section 2.2.1), without strip micro-discharge breakdown [6] and this has been verified by sampling measurements. The initial sensor leakage currents on delivery are, however, specified only up to 350 V, and ~ 1.5 % of sensors have some micro-discharge between 350 V and 500 V in their initial state. This micro-discharge arises from the initial high electric field region close to the edges of the implanted strips in the sensors causing local breakdown, which rapidly decays with time, the plateau value of the current being similar to that for a normal sensor. The definition of acceptable micro-discharge (as opposed to other mechanisms, such as bonding damage, resulting in high currents) used by the SCT is that the current approaches a plateau of less than 1 μA within an hour when held under bias at the onset of the micro-discharge voltage.

The presence of micro-discharge between 350 V and 500 V bias has no implication for the operation of a module at the initial bias of 150 V within ATLAS. However, modules need to be tested during the assembly of the SCT up to their final bias voltage anticipated after 10 years of ATLAS operation to ensure that there is no high voltage breakdown coming, for example, from conducting debris shorting to ground. Thus the modules are grouped into two electrical categories on the basis of their leakage current characteristics:

(a) *Good for any Barrel* - modules with good IV characteristics (module leakage current for the sum of the four sensors versus bias voltage) up to 500 V bias after construction, which can therefore be tested initially for HV integrity up to 500 V and so are suitable for mounting on the innermost barrels.

(b) *Good for Barrel 5 or Barrel 6* – modules with good IV characteristics up to 350 V (the sensor specification) after construction, but with micro-discharge between 350 V and 500 V. They are not tested for HV integrity above 350 V after mounting on the barrel, and so are suitable for Barrels 5 or 6, where the operating voltage in ATLAS is never expected to exceed 350 V. (In practice, all modules selected for mounting on Barrel 5 could be operated up to 400 V, section 5.)

The criteria in Table 9 relating to bad readout channels are based on the definitions of such channels listed in Table 10.

It should be noted that the excellent quality of the sensors with respect to bad channels and leakage current allow limits to be placed on the modules that are considerably tighter than those indicated by the contractual sensor specification (Table 2).

With the ASICs powered, the difference in the thermistor temperatures on the two sides of the hybrid was required to be $< 2\ ^0$C for a module to be accepted for Barrels 3, 4 or 5. This was a check that the hybrid was properly glued to the beryllia baseboard facings, with a good thermal interface (section 3.2.3). For Barrel 6, the

criterion was relaxed to < 4 $^0$C, because of the less stringent thermal requirements in the region of the lowest radiation levels.

Each module was subjected to a long-term cold test (24 h, at the ATLAS operating temperature of ~0 $^0$C on the hybrid thermistors), and was required to operate stably throughout this period, with the expected analogue and digital performance and leakage current.

Table 9: The electrical specifications of the assembled modules. See text for explanation of the barrel assignments. In addition the module must be digitally functional in all respects.

| Measured Quantity | Limit for an electrically good module |
|---|---|
| Average noise occupancy per channel at 1fC threshold (operating both at temperatures of ~27 $^0$C and 0 $^0$C on the hybrid thermistor) | $5 \times 10^{-4}$ |
| Number of bad readout channels per module (operating both at temperatures of ~27 $^o$C and 0 $^o$C on the hybrid thermistor) | ≤ 15 (1% of total) |
| Number of consecutive bad readout channels on a module | ≤ 7 |
| Strip micro-discharge (see text) | None to 500 V bias for mounting on any ATLAS Barrel |
| | None to 350 V bias for ATLAS Barrel 5 or Barrel 6 only |
| Leakage current at 20 $^o$C and 500 V bias if no micro-discharge | < 4 μA |

Table 10: Channel faults causing the individual channel to be classified as bad in the readout.

| Channel Defect | Criterion |
|---|---|
| Channel is dead in readout (stuck off) | |
| Channel is stuck on | |
| Sensors un-bonded to ASIC channel | ENC < 800 electrons |
| Sensors part-bonded (missing bond between them) | ENC < 950 electrons if hybrid thermistor T < 15$^o$C ; |
| | ENC < 1100 electrons if T > 15$^o$C |
| High noise channel | Channel noise > 1.15 × (mean noise of 128 channels in ASIC) |
| High gain channel | Channel gain > 1.25 × (mean gain of 128 channels in ASIC) |
| Low gain channel | Channel gain < 0.75 × (mean gain of 128 channels in ASIC) |
| High offset channel | Channel offset > (mean offset of 128 channels in ASIC + 80 mV) |
| Low offset channel | Channel offset < (mean offset of 128 channels in ASIC – 80 mV) |
| High noise occupancy channel | Noise occupancy of channel > $5 \times 10^{-4}$ |
| Channel threshold cannot be trimmed | |

## 3. Module assembly procedures

### *3.1. Acceptance of the module components prior to assembly*

#### *3.1.1. Silicon microstrip sensors*

The 10,650 silicon sensors used in the assembly of the SCT barrel modules were all fabricated by Hamamatsu Photonics [9] and delivered over a three year period from 2000 to 2003. They were received by three SCT

Institutes [21], where their quality was checked on a sampling basis, and from there they were forwarded for use at the appropriate module assembly site. A small sample of sensors (~0.3%) was extracted during the series production and irradiated at the CERN PS with 24 GeV/c protons to a fluence of $3\times10^{14}$ /cm$^2$, to confirm that the specifications for performance post-irradiation were continuing to be satisfied (section 2.2.1).

The full sensor QA procedures are described in [7]. Detailed QA was carried out by the supplier, and the results provided for each individual sensor on delivery, both on paper, and also as an upload to the SCT production database [22]. Table 11 summarizes the sensor properties checked against the specification by the supplier and at the Institutes.

In addition, the Institutes carried out occasional diagnostic tests of the sensor interstrip capacitance, interstrip resistance, metal strip resistance, and coupling capacitance between strip metal and strip implant. Results of all these measurements are contained in [7].

The post-irradiation tests of the small sample of irradiated sensors were carried out at –18 $^{o}$C, following a seven day anneal at 25 $^{o}$C. They included an IV measurement to 500 V, and measurement of strip quality and comparative charge collection efficiency from a $Ru^{106}$ beta source after bonding the sensor to readout electronics [6].

The sensors are of uniformly excellent quality, and fully satisfy all aspects of the SCT specification. They have low, stable leakage currents (typically 150 nA at 350 V bias, at 20 $^{0}$C), and more than 98% of sensors maintain this performance to 500 V bias. Over 99.9% of all readout strips are good.

Table 11: Sensor QA measurements provided by the supplier and checks at the SCT receiving Institutes.

| Sensor Property | Checked by supplier and data provided for every silicon sensor as applicable | Checked by SCT receiving Institute for each sensor | Checked by SCT receiving Institute on a 5% sampling basis |
|---|---|---|---|
| Serial Number, also recorded on scratch pads on sensor | √ | √ | |
| Visual Inspection | √ | √ | |
| Sensor thickness | √ | | √ |
| Substrate identification | √ | | |
| IV data, 10 V steps, with temperature of measurement | √ to 350 V bias | √ to 500 V bias | |
| Leakage current stability over 24 h period at 150 V bias | | | √ |
| List of strip numbers with AC-coupling oxide pinholes with 100 V across the oxide | √ | | √ |
| List of strip numbers with strip metal discontinuities | √ | | √ |
| List of strip numbers with strip metal shorts to neighbours | √ | | √ |
| List of strip numbers with implant breaks | | | √ |
| Polysilicon bias resistor range | √ | | √ |
| List of strip numbers with defective polysilicon bias resistors | | | √ |
| Depletion voltage | √ | | √ |

### *3.1.2. Baseboards*

The baseboards were fabricated to the specifications given in section 2.2.2, and were subject to the following quality assurance checks before dispatch to the module assembly sites:

- visual inspection for mechanical integrity;
- thickness measurements in both the central region used for sensor interfacing, and in the regions of the large and small beryllia facings (see Fig. 14, the means and standard deviations of the distributions are 430 ±10 μm and 930 ±12 μm, respectively);
- general flatness;
- washer hole diameters, and washer-to-washer separation;
- electrical conductivity of the epoxy-filled facing holes for the sensor backplane bias connections (resistance < 3 Ω);

- electrical conductivity to the substrate of the openings in the encapsulation required for sensor backplane connections.

There were also checks for thermal integrity by monitoring thermal profiles on a sampling basis throughout the series production of nearly 3,000 baseboards [14]. This was done using dummy heat loads and an externally cooled heat sink attached to the large facings. It allowed checks to be made of the thermal conductivity of the graphite substrate and the thermal interface between the substrate core and the beryllia facings. All results were satisfactory, with thermal conductivities measured to be within the specified range.

After these quality assurance checks, the baseboards were transported to module assembly sites in customized solid boxes that provided protection against external impact. At the module assembly sites, each baseboard was inspected by microscope to check for damage, and again for acceptable flatness, and to ensure that washer separations and hole sizes were compatible with site-specific assembly jigging. After satisfying these checks a baseboard was available for use in the first stage of module assembly, namely the assembly of four silicon sensors with one baseboard to form a sensor-baseboard sandwich (section 3.2.1).

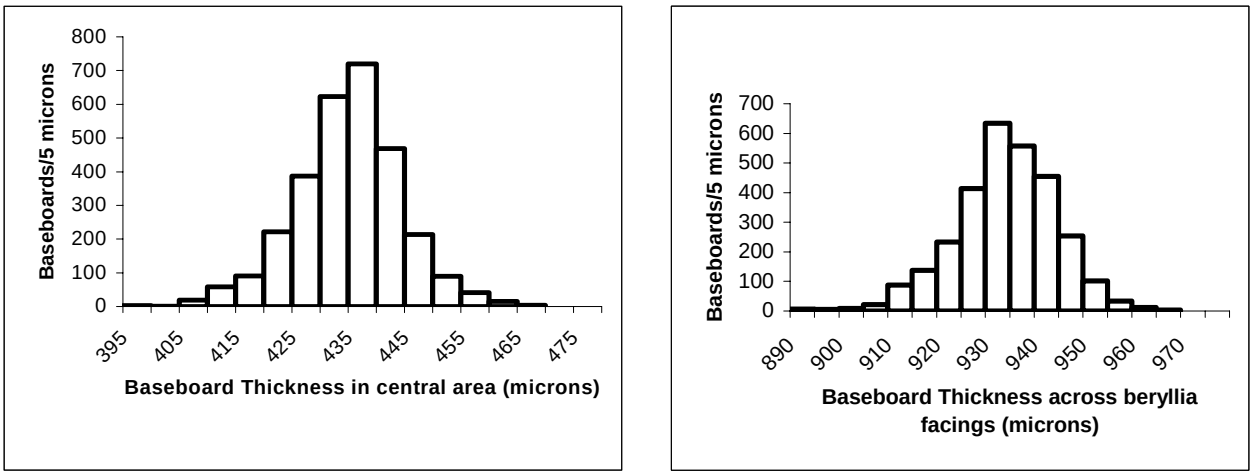



Fig. 14: The measured baseboard thicknesses: left, across the central region of the baseboard and right, across the region of the beryllia facings.

### *3.1.3. Front-end ASICs*

All ABCD3TA ASICs were fully tested at the wafer level at three sites in the SCT collaboration [23]. Full details are given in [8]. The measurements performed included:

- Analogue front-end performance (gain, noise and comparator offsets for every channel);
- Digital functions (control register, addressing, communication, pipeline, output buffer);
- Sensitivity of digital functionality to clock frequency and supply voltage;
- Linearity of internal DACs;
- I/O signal properties (timing, amplitudes, duty cycles);
- Power consumption.

The wafers were diced in industry after measurement, and the good ASICs picked for use in module production.

It was not practical to screen for infant mortality at the wafer level or prior to assembly of the ASICs onto hybrids. However, an extended electrical test was performed on each assembled hybrid and the few ASICs that failed were replaced at that stage, prior to assembly into modules (section 3.2.2).

The radiation hardness of each fabrication lot of ASICs was certified by the foundry based upon their X-ray testing of process monitor devices on a sample of wafers from each lot. As part of the SCT quality assurance (QA) programme, X-ray and neutron irradiations were performed on a small sample of ASICs from each lot to the full radiation specification. Electrical tests were performed after the irradiations and the lot qualified based upon the sample results. Details of the QA programme can be found in [8].

The yield of perfect ASICs on the wafers was only around 20%. The large majority (~ 88%) of the barrel modules were constructed using 12 perfect ASICs, but because of the low ASIC yield, the remaining ~ 12% of

barrel modules were made with some of the 12 ASICs having 1 bad analogue channel flagged in the wafer test, out of the 128 channels.

*3.1.4. Hybrids*

The barrel hybrids and their components were subject to the quality assurance steps described below before being delivered to the module assembly clusters with their passive components mounted.

The Cu/Polyimide flexible circuits were produced according to the specification described in the section 2.2.4 [24]. QA was carried out by the vendor as follows:

- visual inspection for all circuits;
- sampling tests for mechanical tolerance on the outer dimensions, bonding pads/gap widths, plating thickness;
- integrity tests of lines: open/short tests for all circuits, and resistance measurements for samples.

The carbon-carbon (CC) bridges were delivered as a finished product [25]. QA was carried out by the vendor for:

- mechanical tolerance of the outer dimensions;
- the Young's modulus and tensile strength for samples to be greater than 90% of the specified values;
- thermal conductivity of the material to be greater than 600 W/m K;
- electrical resistance less than 25 mΩ between the two farthest openings.

QA on the Al-glass pitch-adapters covered:

- visual inspection for mechanical finish and tolerance, and for opens/shorts of the traces for all pitch adapters;
- tape-peel test of the aluminium traces on a sampling basis;
- wire-bond pull strength test on a sampling basis, with the requirement for the pull strength to be > 6 g for a bond height/distance ratio (H/L) setting of 30%.

The Cu/Polyimide/CC hybrids were assembled and tested in industry [26]. The first process was to glue the CC bridges to the Cu/Polyimide flexible circuits. The QA checks were:

- visual inspection for excess adhesives, residues on the surface, and mechanical tolerance for alignment and thickness, for all pieces;
- bows of the hybrid section at room temperature, to be < 75 μm in both the longitudinal and transverse directions, for all pieces.

The second process was to solder on the surface-mount components (SMD) and the connector, and to attach the two pitch-adapters with glue. The SMD components were soldered manually because it was necessary to avoid high temperature processes (> 60 $^{o}$C) after the gluing of the flexible circuit to the CC bridges. The QA steps carried out for all hybrids were:

- visual inspection for component placement, solder fillets, surface contamination and residues;
- electrical measurement from the connector of the termination resistances and the capacitances between the analogue and digital voltages and their grounds;
- a wire-bond pull test using test pads placed for this purpose, with the requirement of a pull strength of > 6 g for a 30% H/L ratio setting.

After delivery, the finished product (termed a PC-Hybrid) was thermally cycled five times between −20 $^{o}$C and +50 $^{o}$C. Following this, the QA checks were:

- visual inspection for component loss, cracks;
- mechanical tolerances for thickness and bows;
- electrical tests of resistance, capacitance and leakage current in low and high voltage lines, the latter at 500 V.

The tested PC-Hybrids were distributed to the hybrid assembly sites [27]. Upon receipt, visual inspection was made to check for transport damage. Pull tests of aluminium wire-bonding on hybrid gold pads and on the aluminium pitch-adapter pads were made. The minimum pull strength for acceptance was again 6 g for the 30% H/L ratio setting. There were significant problems with the quality and bondability of the aluminium on the glass pitch adapters during the early series production of these pieces, with whiskers being produced around the wire-bonding feet. After lengthy investigation, this was found to be correlated with the hardness of the aluminium. The problem was solved by keeping the temperature of the glass low during the metallization, as

described in [15], and the quality of the delivered product remained high throughout the remaining production. However, the initial pitch adapter problem proved to be the limiting factor in the rate at which barrel modules could be completed.

### *3.2. The Assembly of the module components*

The components were delivered to four clusters [28] for their assembly into modules and for the tests of the completed modules. All assembly work was carried out in clean rooms, of class 10,000 or better. The modules were built to the same specification by all four clusters. The assembly tooling followed common principles, but varied in detail between the clusters in order to make best use of available local infrastructure.

#### *3.2.1. Assembly of sensor-baseboard sandwiches*

This was the process demanding the highest level of mechanical precision. A pair of sensors was aligned in the X-Y plane on the top surface and another pair on the bottom surface of the baseboard. The sensors were aligned relative to one another and to the module reference points, which were the washer dowel holes in the baseboard (section 3.1.2). In this process, it was essential to prevent any mechanical damage to the sensors, and important to minimize distortions out of the X-Y plane, i.e. in the Z direction.

The assembly procedure was based upon having a precision assembly station. This was equipped with two sets of (X, Y, theta) stages to move the two individual sensors on one side, with a large (X, Y) stage to move the sets of (X, Y, theta) stages, and with microscopes. A pair of sensors was aligned to the pre-determined "module physics centre" (section 2.3.1) that was defined relative to the dowel holes of the baseboard. After the sensor pair was aligned, it was transferred to a pick-up jig with vacuum chucking. The alignment precision was preserved during the transfer by switching the vacuum off the stages of the assembly station and the transfer jig, sequentially, to avoid asymmetric forces on the (X, Y, theta) stages. The positions of the sensors in the pick-up jigs were confirmed through inspection holes in the pick-up jigs before and after the transfer. The surfaces of the silicon sensors were protected at all times when in contact with jigs by the use of clean-room paper that was renewed for each separate operation. The design details of the assembly stations were separately optimized by each of the four SCT barrel clusters.

The sensors and the baseboard were glued with thermally conductive epoxy (section 2.2.5). A pre-defined volume of the epoxy was applied to the baseboard to ensure a final glue thickness close to 80 μm, using a glue dispensing machine. In addition, there were two spots per sensor where electrical connection was made between the baseboard and the backside of the sensor through electrically conductive epoxy (2.2.5).

The sensors in the module were numbered as 1 and 2 on the top (link0) side, and 3 and 4 on the bottom (link1) side. Longitudinally, the bridging hybrid overlapped sensors 2 and 4 (Fig. 2). The four sensors in a module were matched according to their properties, such as the wafer orientation <111> or <100>, pre-series or series sensors, and those without or with microdischarge (section 2.3.4). Those sensors with the smallest number of defective strips were used as sensors 2 and 4 in order to maximize the strip area in case the wire-bonding to the defective strips had to be removed in the daisy-chain between the sensors (the ASICs were bonded to the strips of sensors 2 and 4). A full set of (X,Y) metrology survey measurements was performed on the sensor-baseboard sandwich, and the assembly was classified according to the mechanical specifications (section 3.3).

#### *3.2.2. Assembly of ASICs to hybrids*

The ASICs were attached to their pads on the hybrid (Fig. 6) with electrically conductive epoxy [18] for good thermal and electrical contact, although the ASICs were in fact AC-coupled electrically to the pads because their back surface was not metallized. The procedure was to apply the correct amount of epoxy in a defined pattern with a dispensing tool, to align the ASICs by using four fiducial marks at the corners of the chip pads, and to press down the ASICs to provide uniform glue coverage over their full area, with a smooth fillet extending up their sides. The bonding pads near the ASICs were masked to prevent contamination. After the epoxy was cured, the electrical connections on the hybrid (other than to the input pads) were made by aluminium wire-bonding. At this stage, a visual inspection and electrical tests were made on the hybrid to ensure that all ASICs performed to specification and all wire-bonds were functional. The electrical performance of the ASICs was characterized at room (27 $^{o}$C), warm (37 $^{o}$C) and cold (0 $^{o}$C) temperatures, as measured by the thermistors on the hybrids. A temperature of 0 $^{o}$C on the hybrid corresponds to the operating point anticipated within ATLAS.

In addition to the full ASIC characterization on the hybrids, a test of longer duration was performed. The aim of this long-term test was to catch infant mortality problems in the ASICs. The test consisted of a long run at the highest and lowest temperatures, initially 90 h at 37 $^{o}$C and 10 h at 0 $^{o}$C. As no failure was found in the first ~ 300 hybrids tested, the time was subsequently reduced to 10 hrs at 37 $^{o}$C and 10 hrs at 0 $^{o}$C.

In the characterization, the ASICs were powered and triggered at the nominal ATLAS Level 1 Trigger frequency of 100 kHz. The currents drawn and the temperatures were monitored every few minutes. In the long-term test, the currents and temperatures were monitored and the functionality of the ASICs was tested every few hours so that the time structure of any failure could be observed.

An ASIC could be replaced on the hybrid if it had been damaged or if its electrical performance was unsatisfactory. The ASIC was heated, and when the epoxy was softened a twist was applied and the ASIC was detached. A total of 1.3% of the ASICs (affecting 11% of hybrids) were replaced in this manner, and the remainder all performed as expected from the measurements made on the wafer (section 3.1.3).

The 2550 completed hybrids with ASICs (called "ASIC-Hybrids") consisted of two types; the large majority made with 12 perfect ASICs (~ 88% of the total), and the remainder with some of the 12 ASICs having 1 bad analogue channel (section 3.1.3). The assembly and test of the barrel ASIC-Hybrids was carried out at three of the four SCT barrel module clusters [27].

### *3.2.3. Mounting hybrids on to sensor-baseboard sandwiches*

The hybrid is wrapped around the sensor-baseboard sandwich, with the feet of its carbon-carbon bridge attached to the baseboard facings. The procedure was to hold a complete ASIC-Hybrid in a folding jig. The function of the jig was to apply a controlled volume of thermally conductive epoxy (section 2.2.5) to the feet of the link0 hybrid, to align the hybrid to the top surface of the sensor-baseboard by using the fiducial marks on the hybrid surface, to press the hybrid so that the epoxy extended over the area of the foot and formed a smooth fillet at its side, and finally to hold the assembly until the epoxy was cured. The same procedure was repeated for the second side, with the link1 hybrid folded over the bottom side of the sensor-baseboard assembly.

### *3.2.4. Wire-bonding the modules*

The electrical connections were made between the hybrids and the sensors in two stages, using 25 μm aluminium wire with ultrasonic wire-bonding. Firstly, the high-voltage bias supply and high-voltage return connections were made between the hybrid and the sensor-baseboard. The bias supply connections were made to the gold pads on the upper-side beryllia facings (section 2.2.2). These pads connected the bias supply to the graphite of the baseboard, and from there to the backside of the sensors via the holes in the encapsulation and the electrically conducting epoxy. At least four bond-wires were used for each connection to the large and to the small facings, to provide redundancy. The bias return connections were made by wire-bonding from the hybrid to the bias ring pads of the sensors. At least two wire-bonds were made at each of two points in both the upper and the lower sensors, again for reasons of redundancy. The leakage current of the sensors was measured up to 500 V at this stage on a regular sampling basis, to check that the assembly process was not damaging the sensors.

Secondly, the high-density wire-bonds were made from the ASICs to the pitch-adapters, if this had not been done at the ASIC-Hybrid stage, from the pitch adapters to the sensors, and between the daisy-chained strips of the two sensors. There were a total of 4608 wire-bonds per module, which took two to three hours to complete, using automatic bonding machines. All strips of the sensors were wire-bonded to the pitch-adapters, and thus to the ASICs, irrespective of any defects in the strips.

## *3.3. Module metrology measurements during assembly*

The completed sensor-baseboard assemblies, and then the modules, were surveyed for mechanical precision. The module was held by vacuum in a measurement frame at three points. The precision was characterized by in-plane and out-of-plane parameters. For the in-plane survey, a well-defined set of fiducial marks on the sensors was used. For the out-of-plane survey, a matrix of points was measured on the surface of the sensors and the beryllia facings. The coordinate systems of the upper and the lower measurement were correlated by the measurement of a number of reference points observable both from the upper and the lower sides, for example, transparent fiducial marks on the frame, or corner edges of the upper and lower sensors. The location of the connector on the pigtail section of the hybrid was critical for mating the connectors on the barrels (Fig. 11). The measurement of the hybrid position defined the location of pin number 1 of the connector for the ideal case of a

flat and straight pigtail. A three-dimensional (3D) measuring machine was used for the survey at each cluster, and the results were uploaded to the SCT production database [22].

*3.3.1. In-Plane (XY) Survey*

The in-plane survey characterizes the relative positions of the four sensors and the dowel hole and slot of the baseboard washers, which define the module position on the barrel. The X and Y coordinates of a sensor were obtained from the measurement of eight fiducial marks on a sensor, 1 to 16 and 51 to 66 in Fig. 15. The reduced parameter set used (Fig. 16) did not, however, rely on this choice of fiducial marks. The centres of the dowel hole and slot were obtained from the measurement of perimeters of the respective washers from the upper side. From the (X,Y) coordinates measured, a reduced parameter set was obtained as shown in Fig. 16. The origin of coordinates was the geometrical centre of the four sensors, the "module physics centre". C1 to C4 were the geometrical centres of the fiducial marks of the sensors 1 to 4, respectively. The stereo angle was the angle between the axes of the front pair, C1 and C2, and the back pair, C3 and C4. The centre-line along the X direction of points C1, C2, C3, and C4 was the X-coordinate, $X_m$. The reduced parameter set is summarized in Table 12, with the design values and the tolerance specifications. The positions of the hybrids were measured using two fiducial marks on each on the hybrids (link0 and link1). The link0 position was used to deduce the connector position in the pigtail.

*3.3.2. Out-of-Plane (Z) Survey*

The out-of-plane module tolerances are constrained by two factors. One is the requirement to keep the separation between the surfaces of adjacent modules on a barrel to be at least 1 mm (section 2.3.1). This sets the maximum deviation of sensor surfaces from the nominal to be < 200 μm. The other requirement relates to the deviation in flatness of a module. This arises because z and r-phi measurements are correlated on a barrel because modules are mounted at a tilt angle of approximately $11^0$ (Table 1). This sets the deviation in Z-flatness to be <70 μm from the expected value, if the r-phi resolution is not to be compromised.

The Z-coordinates of the surfaces of the sensors were measured on the front and back of the module using 3D measuring machines having a Z-precision of better than 10 μm. The upper and lower surface Z-coordinate systems were tied together through the measurement taken around the points 1, 7, 11, 13, 51, 57, 61, and 63 of Fig. 15 at the corners of the sensors. These were visible on the two sides of the sensor because of the stereo rotation and displacement, and were taken to be 285 μm apart in Z, the nominal thickness of the sensors. The module plane was defined from the Z-coordinates of the three surface areas on the lower side of the facings around the dowel hole, the dowel slot, and the third mounting point on the small facing. The surfaces of each sensor were measured at the matrix of 5 x 5 points in Fig. 15. The measurement points in the areas of columns 9-15 and 10-14 on the front side, and 59-65 and 60-64 on the back side, were obscured by the hybrid on the module, and their sensor Z-coordinates were inferred by interpolation from neighbouring points.

The maximum deviation of the sensor surfaces from the nominal was obtained directly from the surface measurements. Individual modules are not expected to be flat to within 70 μm, because of the intrinsic bows of the sensors. Instead, the requirement was that the shape of an individual module differed by < 70 μm from a standard ‘common profile’, which was obtained from the average of the measurements of the constructed modules. The use of a common profile was a good method to ensure the stability of the construction process.

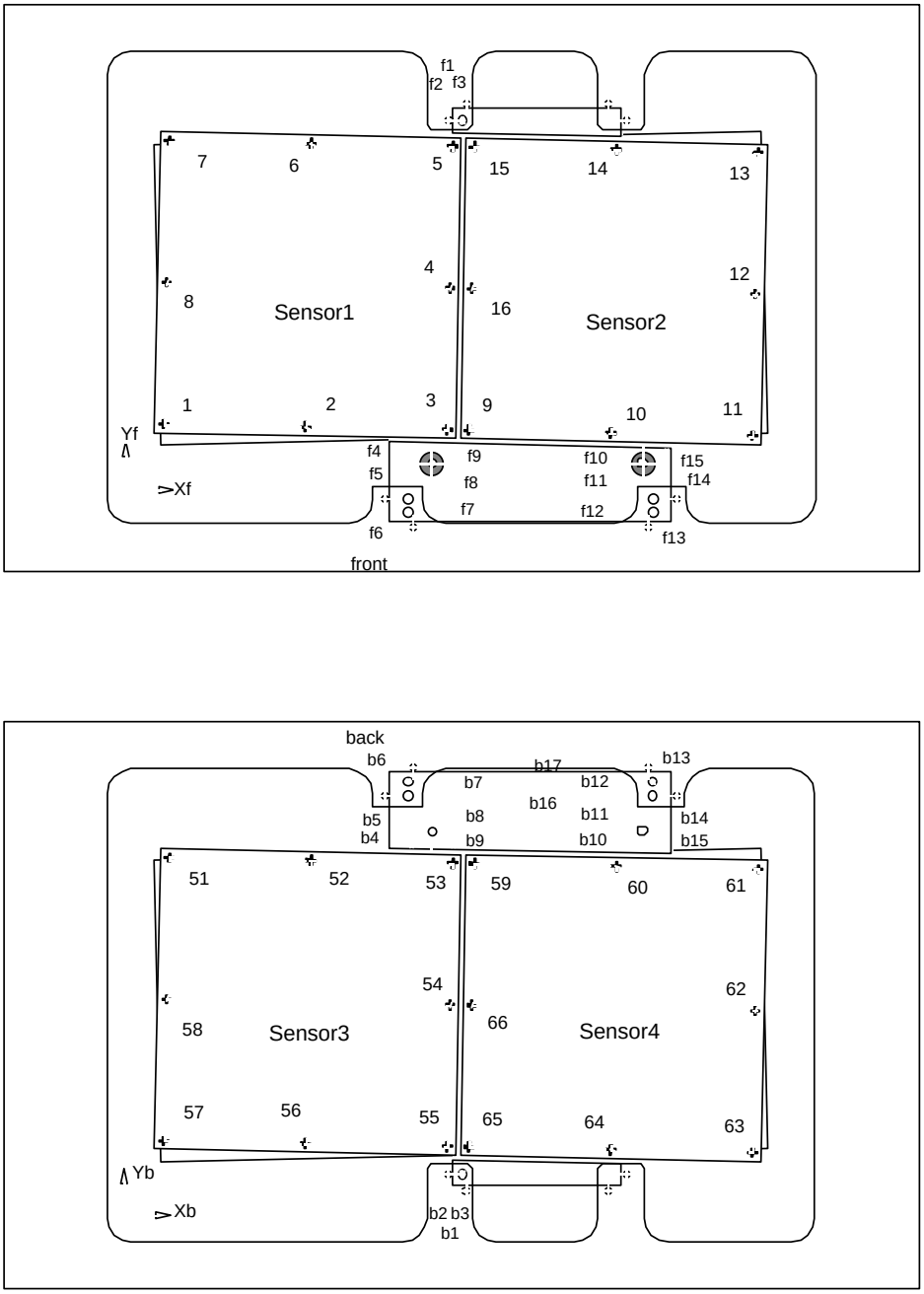



Fig. 15: A survey frame and the survey points of the SCT barrel module (hybrid is not shown in the figure). Sensors 1 and 2 are on the top (link0) side and 3 and 4 the bottom (link1) side. Sensors 1 and 3 are on the left when the module is held in the conventional orientation (i.e., hybrid on the right side). The mark "+" represents the fiducial marks on the sensors. Points 1-16 and 51-66 are for the in-plane survey. For the out-of-plane survey, points on a 5x5 matrix were measured for a sensor. The survey frame has "peepholes" in the arms for the cooling facing and for the 3rd mounting point in the small facing (section 2.2.2). The arm opposite to the 3rd mounting point was retracted in height so that the module was held kinematically at the three points used to mount the module on a barrel.

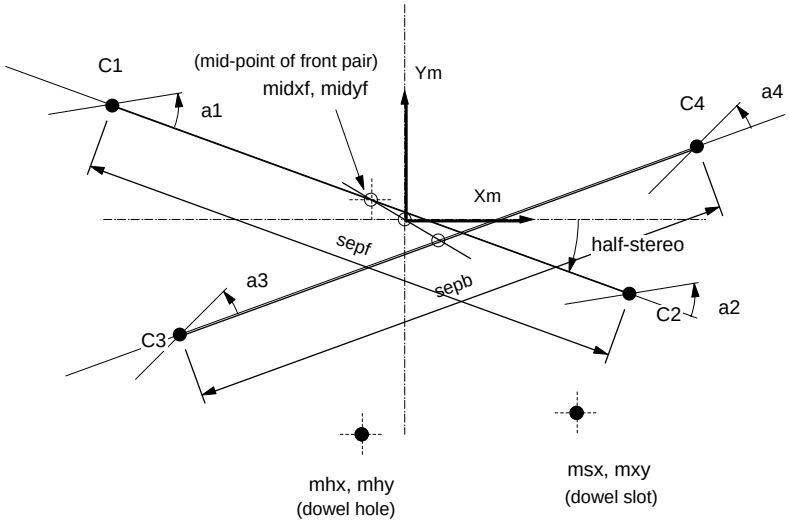



Fig. 16: In-plane parameters of the SCT barrel module. The black circles, C1 to C4, are the geometrical centres of sensors. The origin of the coordinates is the geometrical centre of the C1 to C4, the "module physics centre". The line connecting C1 to C2 is the axis of the upper (front) sensors, and the line C3 to C4 the lower (back) sensors. The open circles are the centres of the pairs. The offset of the front and the back pairs is defined by the coordinates (midxf, midyf) of the front pair. The orientations of individual sensors, a1 to a4, are defined from the axes of the pairs.

Table 12: In-plane parameters of the SCT barrel module.

| Parameter | Design Value | Specified Tolerance |
|---|---|---|
| Dowel hole, mhx [μm] | −6500.0 | 40.0 |
| Dowel hole, mhy [μm] | −6500.0 | 40.0 |
| Dowel slot, msx [μm] | 38500.0 | 140.0 |
| Dowel slot, msy [μm] | −37000.0 | 40.0 |
| Mid-point of front pair, midxf [μm] | 0.0 | 20.0 |
| Mid-point of front pair, midyf [μm] | 0.0 | 8.0 |
| Separation of front pair, sepf [μm] | 64090.0 | 20.0 |
| Separation of back pair, sepb [μm] | 64090.0 | 20.0 |
| Sensor1 angle, a1 [mrad] | 0.00 | 0.13 |
| Sensor2 angle, a2 [mrad] | 0.00 | 0.13 |
| Sensor3 angle, a3 [mrad] | 0.00 | 0.13 |
| Sensor4 angle, a4 [mrad] | 0.00 | 0.13 |
| Half stereo angle, half-stereo [mrad] | −20.00 | 0.13 |
| Mid-point of front hybrid fiducial pair, hymxf [μm] | 7698.5 | 200.0 |
| Mid-point of front hybrid fiducial pair, hymyf [μm] | −154.0 | 200.0 |
| Angle of front hybrid fiducial pair, hymaf [mrad] | −20.00 | 3.145 |
| Mid-point of back hybrid fiducial pair, hymxb[μm] | 7698.5 | 200.0 |
| Mid-point of back hybrid fiducial pair, hymyb [μm] | 154.0 | 200.0 |
| Angle of back hybrid fiducial pair, hymab [mrad] | 20.00 | 3.145 |
| Connector pin #1, conp1x [μm] | 3611.8 | 480 |
| Connector pin #1, conp1y [μm] | −69451.1 | 200 |

The surface of an individual module was parameterised in the following way:

(1) The *midplanes* in Z of the left and the right sensors were the average of the planes of the surfaces of the upper and lower sensors in the left and the right sides of the module. These two (left, right) *midplanes* were each fitted separately to the equation $Z = aX + bY + c$. The two sets of (*a, b, c*) parameters express any asymmetry in the construction of the module, or non-planar properties of the baseboard.

(2) The *module thickness* was defined by the average distance between the surfaces of upper and lower sensors over the area covered by the baseboard.

(3) *Common profile*: The bowing of the sensors on an individual module is given by the deviations of the 100 measured points from the module *midplanes,* having subtracted half the *module thickness.* The average of these 100 deviations for the constructed modules defined the *common profile* of the sensor surfaces. Since the bowing of the sensors is different for the two types of wafer orientation used, <111> and <100> silicon, separate c*ommon profiles* were used for the <111> and <100> modules. That for the upper surface of <111> modules is shown in Fig. 17.

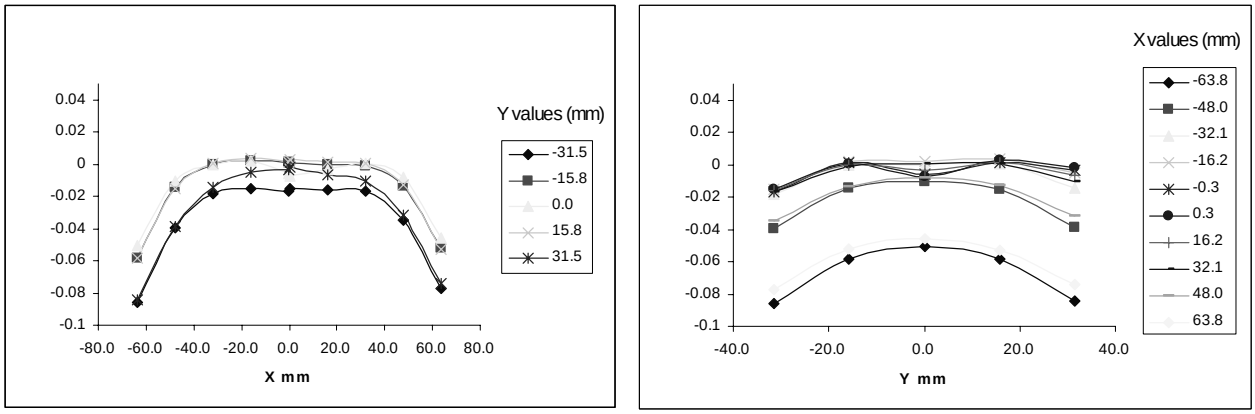



Fig. 17: The common Z profile (in mm) of the surface of the upper sensors for <111> modules (see text). The lower surface is very similar, but with the opposite sign of Z. The left figure shows the profile along the length of the module (X), at different transverse positions (Y), and the right figure the profile across the module (Y) at different longitudinal positions (X).

(4) *optimalMaxZerror* and *optimalRMSZerror*: After the above parameterization, the residuals from the *common profile* were the errors in Z-flatness for an individual module. The maximum residual was called *optimalMaxZerror* and the r.m.s. of the residuals *optimalRMSZerror*. In the subsequent reconstruction of tracks in ATLAS, the sensor surface of the *i*-th of the 2112 barrel modules, *Z(X,Y: surface, side, i)*, can be obtained within these errors from the 100 points of the *common profile,* $Z_{CP}(X, Y:surface)$, the individual *module thickness, T(i),* and the *Midplane* equation with the parameters (*a, b, c*) of the left and right side, $Z_{MID}(X, Y: side, i)$:

$$Z(X,Y: surface, side,i) = Z_{CP}(X, Y: surface) + Z_{MID}(X, Y: side, i) \pm T(i)/2 \quad (2)$$

where the surface and side denote the upper or lower surface and the left or right side, respectively, and the ± is for the upper/lower surface.

Further relevant parameters were obtained from the surface measurements, in addition to the sensor shapes. The surfaces of the far-end and the cooling beryllia facings were measured at 17 and 15 points, b1 to b17 on the lower side and f1 to f15 on the upper side, respectively (Fig. 15). The upper side has two points less where the pigtail of the hybrid hides the surface. The third mounting point was measured at three neighbouring points, b1 to b3 in Fig. 15, to increase the accuracy. These measurements gave the thickness of the baseboard tabs. The hole and slot area surfaces were measured at four points each: b4, b5, b8 and b9, and b10, b11, b14, and b15. These points are 2 mm away from the hole/slot washers so that the fillet of adhesive around the washers did not affect the measurement. The average of (b4, b5, b8, b9) defined the Z-coordinate of the hole, Z1, the average of (b10, b11, b14, b15) the Z-coordinate of the slot, Z2, and the average of (b1, b2, b3) the Z-coordinate of the third mounting point, Z3. These Z1, Z2, and Z3 defined the lower cooling facing plane, *LoCoolingFacing*, and by adding half the tab thickness, the *Moduleplane*. The difference of the Z-coordinates of the centre of the tabs and the centre of the sensor-baseboard allows any asymmetry in the thickness of the adhesive gluing the sensors to the upper and the lower sides of the baseboard to be monitored. The angle of the lower beryllia cooling facing

across the module is an important parameter, since this facing has to make good thermal contact, via thermal grease, with a flat cooling block when the module is mounted on the cylinder.

Parts of the module envelope were critical for mounting the modules on the support cylinders. The most critical components were the three large capacitors on the hybrid near the far-end tab. The surface measurement of the hybrids and the capacitors gave the envelope. In addition, these measurements showed the heights of the hybrids at the tabs, and thus the thickness of the adhesives attaching the hybrids to the facings. This thickness needed to be well controlled, both for thermal and for mechanical reasons.

The principal module Z parameters derived from the measurement of the sensors, the tabs and the hybrids are summarized in Table 13, together with the nominal values and tolerance specifications.

Table 13: Z parameters of the SCT barrel module.

| Parameters | Nominal | Tolerance | Description |
|---|---|---|---|
| maxZlower [mm] | 0 | abs < 0.2 | lower sensor maximum deviation from ModulePlane |
| maxZupper [mm] | 0 | abs < 0.2 | upper sensor maximum deviation from ModulePlane |
| moduleThickness [mm] | 1.15 | diff < 0.1 | |
| optimalMaxZerrorLower [mm] | 0 | abs < 0.07 | lower sensor maximum deviation from CommonProfile |
| optimalMaxZerrorUpper [mm] | 0 | abs < 0.07 | upper sensor maximum deviation from CommonProfile |
| optimalRmsZerrorLower [mm] | 0 | abs < 0.025 | lower sensor RMS deviation from CommonProfile |
| optimalRmsZerrorUpper [mm] | 0 | abs < 0.025 | upper sensor RMS deviation from CommonProfile |
| coolingTabThickness [mm] | 0.93 | < 1.0 | cooling-side tab thickness including baseboard and adhesive |
| farTabThickness [mm] | 0.93 | < 1.0 | far-side tab thickness including baseboard and adhesive |
| loCoolingFacing a [mrad] | 0 | abs < 0.5 | lower cooling facing angle along the module, 30 μm over 60 mm |
| loCoolingFacing b [mrad] | 0 | abs < 5 | lower cooling facing angle across the module, 50 μm over 10 mm |
| loCoolingFacingConcavity [mm] | 0 | abs < 0.03 | lower cooling facing concavity along X, 30 μm over dowel hole/slot |
| hyb1NearH [mm] | 1.18 | 0.25 | height of the near-side surface of the upper hybrid from the upper facing |
| hyb1FarH[mm] | 1.18 | 0.25 | height of the far-side surface of the upper hybrid from the upper facing |
| hyb2NearH [mm] | 1.18 | 0.25 | height of the near-side surface of the lower hybrid from the lower facing |
| hyb2FarH [mm] | 1.18 | 0.25 | height of the far-side surface of the lower hybrid from the lower facing |
| hyb1Concavity [mm] | 0 | 0.125 | concavity of the upper hybrid (+ : away from sensors) |
| hyb2Concavity [mm] | 0 | 0.125 | concavity of the lower hybrid (+ : away from sensors) |
| hyb1CapMaxH [mm] | 2.43 | 0.30 | maximum height of the large capacitors, C73, C53, C54, of the upper hybrid from the upper facing |
| hyb2CapMaxH [mm] | 2.43 | 0.30 | maximum height of the large capacitors, C74, C55, C56, of the lower hybrid from the lower facing |
| hybridMaxThickness [mm] | 3.28 | 0.44 | maximum thickness of the module at surface of the hybrid |
| capMaxThickness [mm] | 5.78 | 0.66 | maximum thickness of the module at surface of the large capacitors |

### *3.4. Thermal Cycling*

Every module was thermally cycled ten times from –25 $^{o}$C to +40 $^{o}$C, unpowered, in an inert atmosphere. The module was placed inside an environmental test chamber which was purged with nitrogen for sufficient time to prevent condensation when cold (typically three volume changes within the chamber). The test cycle started and ended at room temperature. The ramp up/down times were approximately 30 minutes (2-3 $^{o}$C/minute) and the soak time about 30 minutes at each temperature. The total test time was about 20 hours.

The module metrology measurements were repeated after the thermal cycling, and compared with their initial values (section 4.2.1).

*3.5. Electrical Tests of Modules*

Each SCT module was housed in its own metal box after assembly and metrology, and remained in this box until removed by a robot during the process of mounting onto an ATLAS barrel. All electrical tests before mounting were carried out with the module in its box. The module was attached to the aluminium of the box through the holes in the larger beryllia facing and a clip at one side of the small facing, as illustrated in Fig. 18. This follows the principle used for attachment to an ATLAS barrel. The module connector was permanently attached to a transition PCB mounted in the box (Fig. 18), to avoid damage due to its repeated use, and the connector used during testing was located at the edge of this PCB. The analogue ground of the hybrid was connected to the metal of the box. The box could be mounted on a water-cooled plate to provide the necessary cooling during 'warm' electrical tests. For these, the temperature of the thermistors attached to the upper and lower faces of the powered module hybrid were typically ~27 $^{o}$C, about 15 $^{o}$C above that of the cooling water. The module box had an inlet gas connection, and all electrical tests were carried out with the module in a dry nitrogen atmosphere. For 'cold' tests, the box was placed in a commercial freezer or a climate cabinet, and operated with the thermistor on the powered hybrid at ~ 0 $^{o}$C.

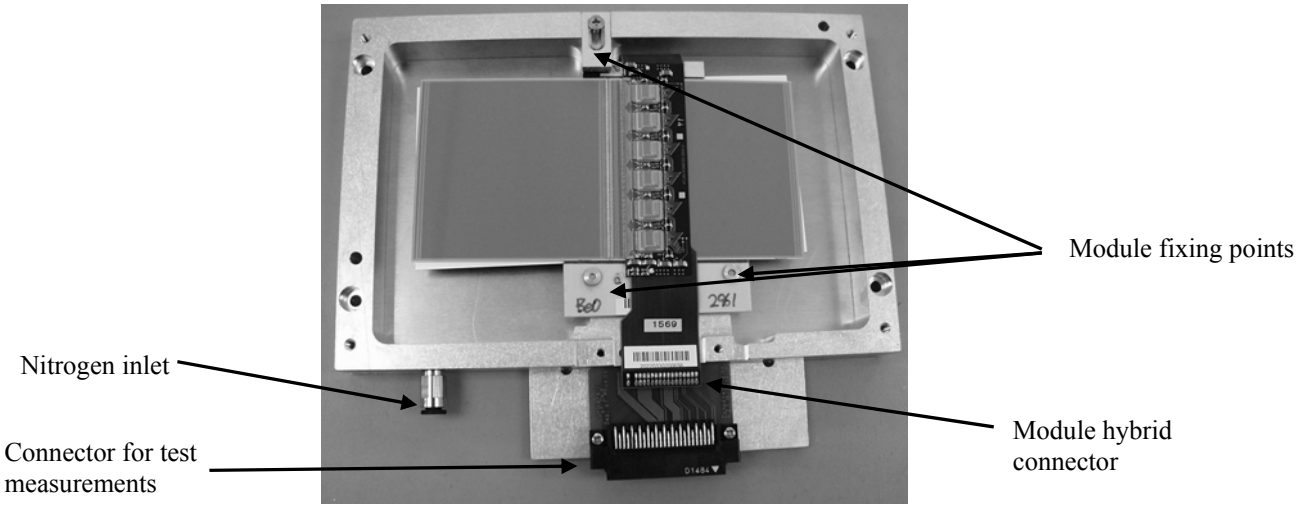



Fig. 18: A module housed within a module test and storage box. A metal plate closes the top of the box.

The individual modules in their boxes were tested using custom readout electronics and low and high voltage power supplies developed by the SCT for these functionality tests [29,30,31,32]. The ABCD3TA ASIC (section 2.2.3) binary readout architecture requires the parameters of the front-end channel to be extracted by performing threshold scans for different amplitudes of injected test pulses, controlled by internal calibration circuitry. For each value of the test charge, the result of the threshold scan is a complementary error function with the 50% point corresponding to the signal amplitude at the discriminator input and the transition width containing information on noise spread. The threshold scans provide a response curve, the discriminator threshold as a function of input charge, for each individual channel. From the error functions, the channel gain, discriminator offset and ENC (equivalent noise charge) at the discriminator input can be extracted. Details of the performance and operation of the ASICs are given in [8].

Each module underwent a warm electrical characterization and acceptance test, and a 24 h cold electrical stability test in the module assembly cluster. The cold test verified that the module would function electrically at the ATLAS operating temperature. The test consisted of an extended run, with the ASICs being clocked and triggered, and with the temperature of the thermistors on the hybrids around 0 °C. All currents were monitored every five minutes, and every few hours a short electrical test was performed. At the end, a full set of electrical tests was performed while the module was kept cold.

All electrical results were uploaded to the central SCT database.

## 4. The performance of the assembled modules

### *4.1. Mechanical precision of the modules*

A selection of typical in-plane (XY) survey results is shown in Fig. 19, and of out-of-plane (Z) survey results in Fig. 20 for all modules, measured at room temperature either after the assembly or after the long-term electrical test. In each figure, the horizontal range of the distribution is the tolerance specification of the quantity, as given in Table 12 and Table 13. Nearly all parameters are well within the specification, and the standard deviations of their measured distributions are less than one-third of the tolerance, as shown in Table 14. In total, 97% of the 2,582 modules entering the sensor-baseboard sandwich assembly step satisfied the complete set of in-plane and out-of-plane mechanical specifications.

### *4.2. Thermal performance of the modules*

#### *4.2.1. Thermally Induced Distortions.*

The changes in the measured parameters before and after the steps of thermal cycling and the long-term cold test have been measured for a subset of modules. The module is very rigid in-plane, and there is no measurable change in any of the in-plane parameters. The module is less constrained mechanically out-of-plane. As illustrated in Fig. 21, the measured changes in the maximum Z deviations after thermal cycling are normally $\leq 10$ μm, and a further change of up to 20 μm may be present after the long-term test. Changes at the 10 μm level are comparable with the measurement errors in Z, but it cannot be excluded that the larger values correspond to real deformations. Nevertheless, these are small in comparison with the tolerances of the out-of-plane mechanical specifications; a maximum Z deviation of $< 200$ μm and the OptimalMaxZerror parameter $< 70$ μm.

Further studies on elastic and non-elastic thermally induced distortions were carried out on mechanical modules. A total of four modules were built, using non-electrically working but thermally realistic components. Each module was heated or cooled over a temperature range of –17 $^{o}$C to +39 $^{o}$C. At five temperatures (−17 $^{o}$C, −6 $^{o}$C, +7 $^{o}$C, +21 $^{o}$C and +39 $^{o}$C) the profile was measured with a 3D measuring machine.

Each module was then thermally cycled ten times between −30 $^{o}$C and +100 $^{o}$C in a nitrogen atmosphere and the profile re-measured. No variations in the in-plane XY measurements were observed. Out-of-plane Z variations were measurable only at the unsupported corners of the detectors. The average movement seen over all temperature variations for the four modules, prior to thermal cycling, was 1.29 μm/$^{o}$C. After thermal cycling, this average value was 1.33 μm/$^{o}$C, that is, essentially unchanged.

The systematic alteration in the out-of-plane shape of the silicon sensors in the module between room temperature measurements and cold operation in ATLAS will be taken into account by applying an appropriate modification to the single parameterized common profile of the modules (section 3.3.2).

#### *4.2.2. Thermo-profile measurement of the hybrid*

The temperature profile was measured for a sample of (un-irradiated) modules by using a thermo viewer. This measurement requires care because of practical difficulties such as:

- estimating or determining the reflectivity of the surface, which depends on the surface and the material;
- shielding against infra-red light from the external environment;
- the infra-red transparency of silicon.

The transparency of silicon to infra-red wavelengths precluded the measurement of the temperature of the silicon sensors. Thus the measurement was only effective for estimating the temperature of the hybrids and the beryllia facings.

A measured temperature profile of the hybrid is shown in Fig. 22, with an ASIC power of 5.3 W. In the figure, the temperatures are given with respect to that of the top surface of the beryllia cooling facing. The highest temperature on the hybrid was 11 – 12 $^{o}$C, at the ASICs. The temperature at the hybrid thermistor was about 6 $^{o}$C. The measurements are consistent with the thermal FEA simulations (section 2.3.2).

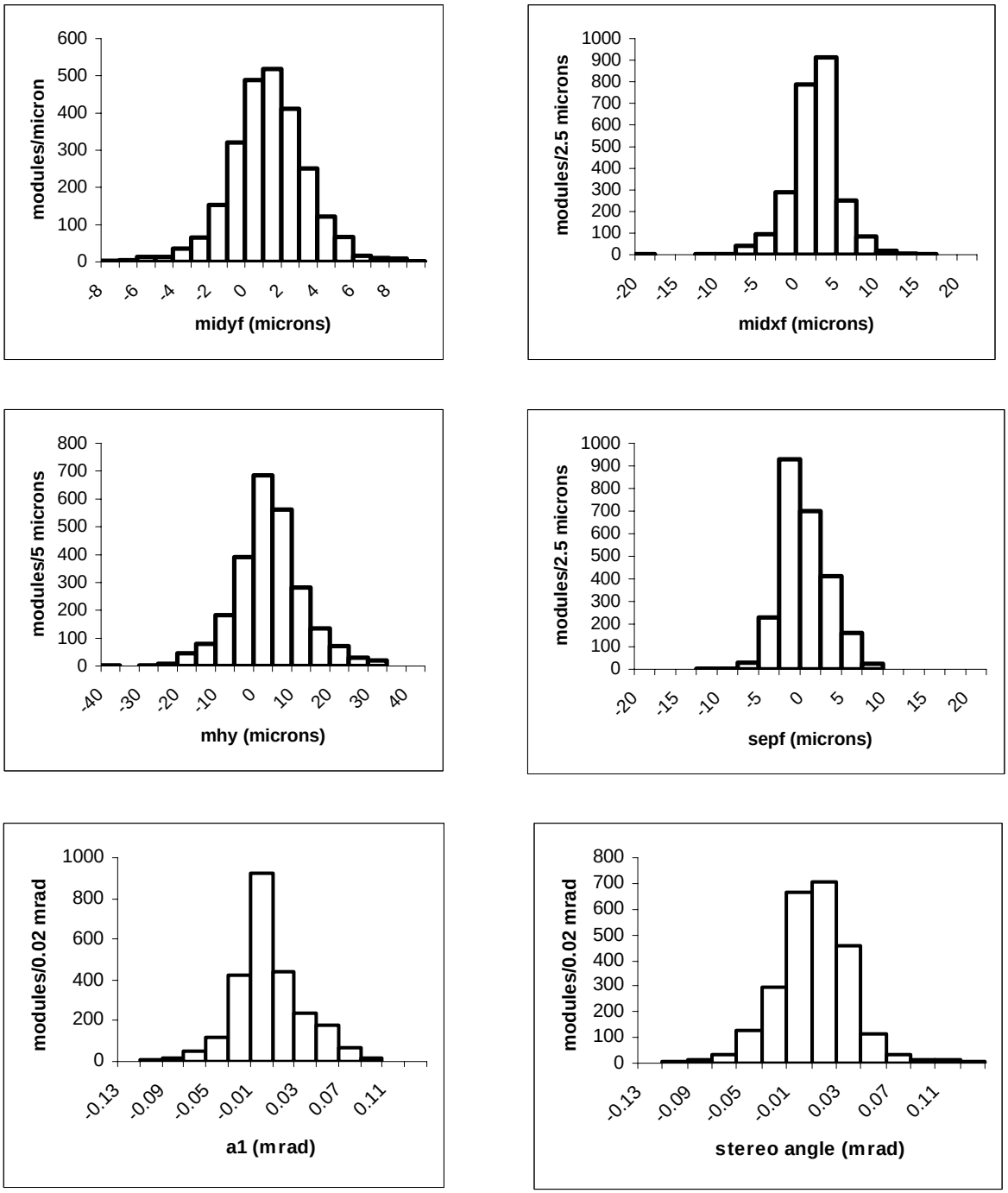



Fig. 19: The measured distributions of the deviations from their design values of a selection of module in-plane metrology parameters, whose definitions are shown in Fig. 16. Each plot is centred about the design value, with width ± the specified tolerance (Table 12). The parameters are, from left to right: top row, midyf, midxf; middle row, mhy, sepf; bottom row, angles a1 and half-stereo.

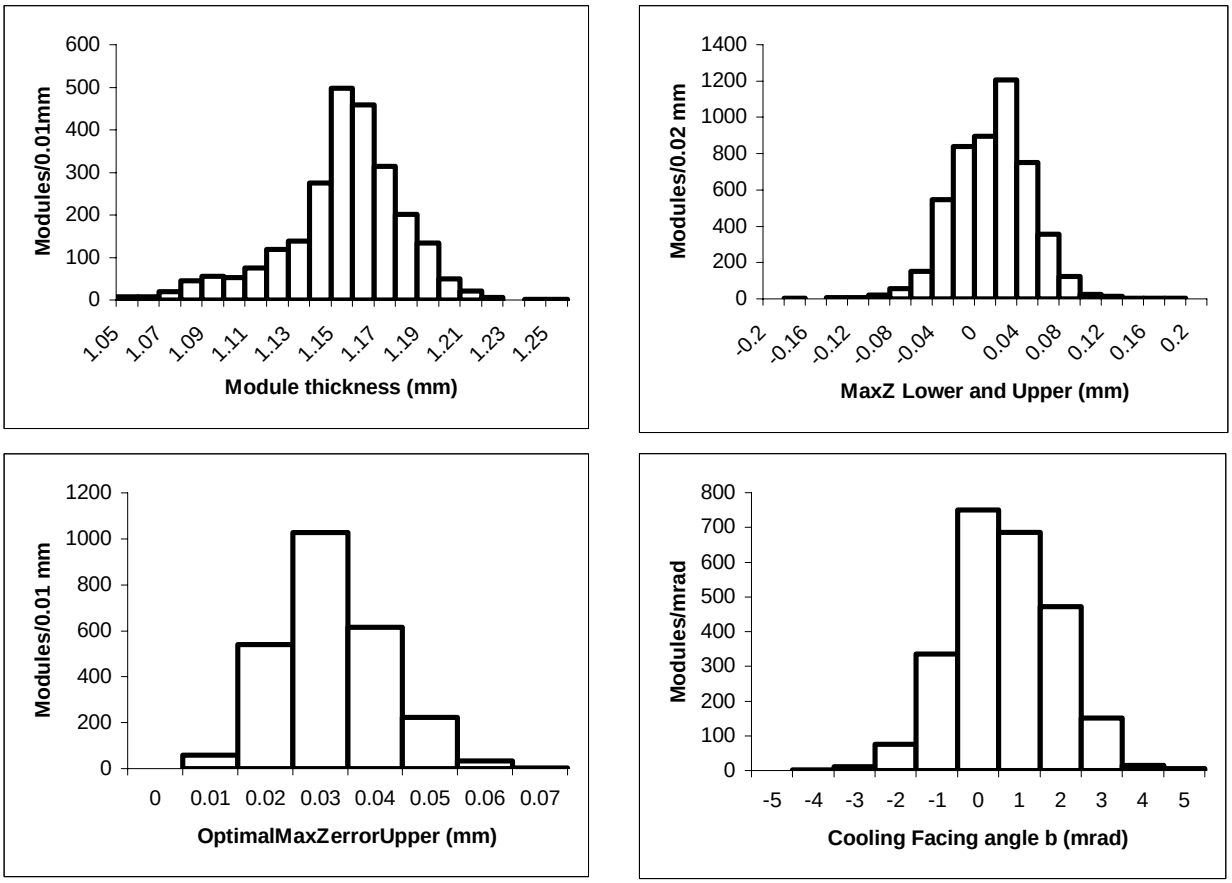



Fig. 20: The measured distributions of a selection of module Z (out-of-plane) metrology parameters, which are defined in Table 13. Each plot is centred about the design value, with width ± the specified tolerance (Table 13). The parameters are, from left to right: top row, module thickness, maxZlower and maxZupper; bottom row, optimalMaxZerrorUpper , loCoolingFacing angle b.

Table 14: The standard deviation of the the measured distributions of mechanical parameters for all modules and their comparison with the specified tolerances.

| XY (in-plane) Parameter | Measured standard deviation | Standard deviation/ Specified tolerance | Z (out-of-plane) Parameter | Measured standard deviation | Standard deviation/ Specified tolerance |
|---|---|---|---|---|---|
| Dowel hole, mhx | 11.0 µm | 0.27 | maxZlower | 0.023 mm | 0.11 |
| Dowel hole, mhy | 9.1 µm | 0.23 | maxZupper | 0.022 mm | 0.11 |
| Dowel slot, msx | 28.3 µm | 0.20 | moduleThickness | 0.033 mm | 0.33 |
| Dowel slot, msy | 11.4 µm | 0.28 | optimalMaxZerrorLower | 0.010 mm | 0.14 |
| Mid-point of front pair, midxf | 3.1 µm | 0.15 | optimalMaxZerrorUpper | 0.010 mm | 0.14 |
| Mid-point of front pair, midyf | 2.2 µm | 0.27 | optimalRmsZerrorLower | 0.004 mm | 0.15 |
| Separation of front pair, sepf | 2.9 µm | 0.14 | optimalRmsZerrorUpper | 0.004 mm | 0.15 |
| Separation of back pair, sepb | 3.0 µm | 0.15 | loCoolingFacing a | 0.145 mrad | 0.29 |
| Sensor angles, a1-a4 | 0.031 mrad | 0.24 | loCoolingFacing b | 1.250 mrad | 0.25 |
| Half stereo angle, half-stereo | 0.030 mrad | 0.23 | loCoolingFacingConcavity | 0.007 mm | 0.22 |

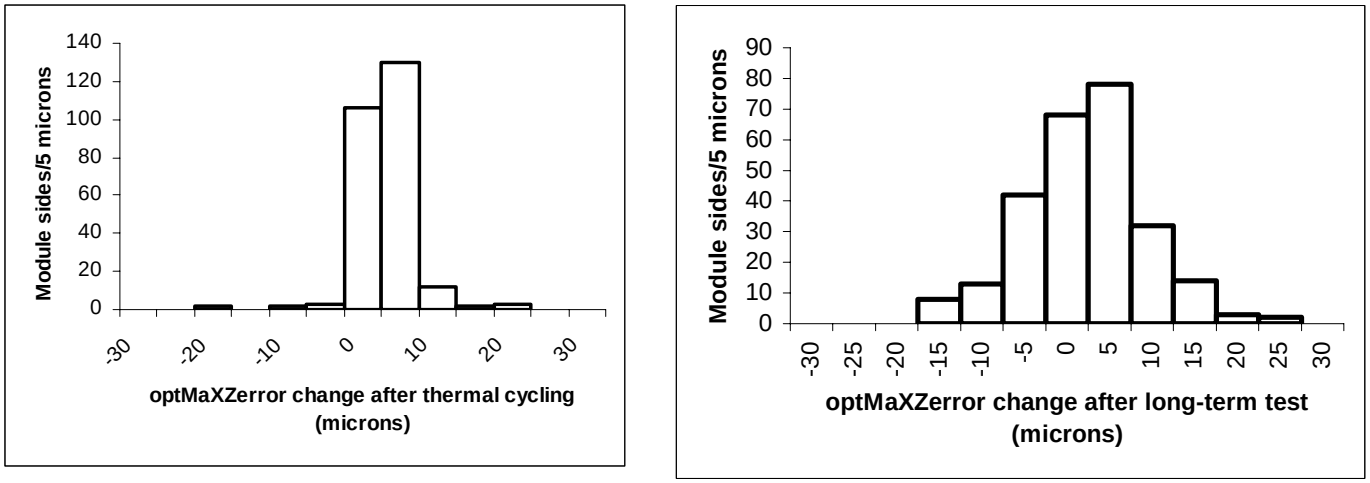



Fig. 21: Changes in module out-of-plane (Z) OptimalMaxZerror parameters after thermal cycling (left) and a cold long-term test (right).

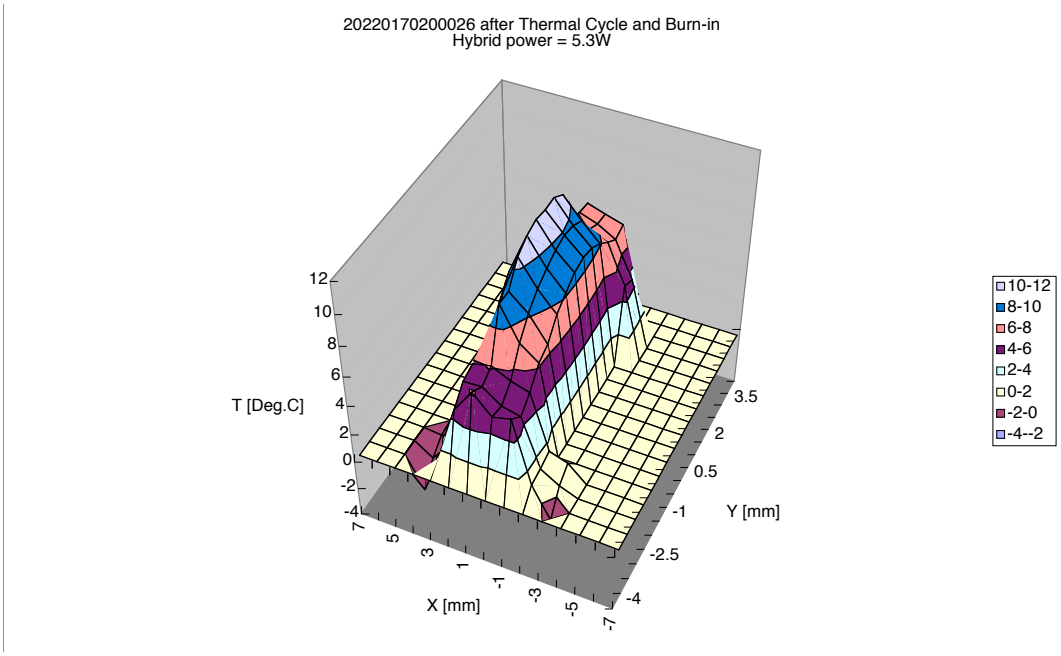



Fig. 22: The temperature profile of a powered hybrid measured using a thermo viewer.

*4.2.3. Thermal runaway measurement*

A thermal module was built using silicon microstrip sensors irradiated to the fluence corresponding to 10 years of LHC operation. The sensors were assembled to a pre-series baseboard and the module was completed by mounting a pre-series Cu/Polyimide/CC hybrid. The heat generated by the ASICs was simulated using 2.2 Ω silicon-chip heaters. The module was equipped with a number of Pt100 thermal sensors that provided temperature readout of the two hybrids, three of the detector corners, the upper cooled facing, the cooling block and the ambient gas temperature. The cooling was provided by a mixture of water and antifreeze flowing in a copper pipe, and the cooling interface was via thermal grease to a copper block brazed to the pipe.

The results showed stable running at a coolant temperature of around –10.5 $^{o}$C with a detector power dissipation of about 130 μW/mm$^2$, normalized to 0 $^{o}$C. The FEA predicted thermal runaway at such a coolant temperature at ~ 135 μW/mm$^2$. Thus the results supported the safety factor against thermal runaway with the envisaged coolant temperatures of ATLAS given by the FEA calculations (section 2.3.2).

### *4.3. Electrical Performance of the Modules*

The electrical acceptance criteria for SCT barrel modules to be classified as good are described in section 2.3.4. Overall, 93.3% of the completed modules satisfied these criteria. The percentages failing to meet the different criteria are summarized in Table 15. The majority of these failing modules are appropriate to keep as spare modules for ATLAS.

Table 15: The percentages of modules failing the electrical specifications

| Good Electrical Acceptance Criterion | % of completed modules failing this criterion |
|---|---|
| Noise occupancy at 1fC threshold < $5\times10^{-4}$ | 0.8% |
| ≤ 15 bad readout channels and ≤ 7 consecutive bad readout channels | 0.7% |
| No strip micro-discharge below 350V bias, leakage current at 500V (or at micro-discharge voltage) < 4 μA | 5.2% |
| Total failing the good electrical criteria | 6.7% |

In the following sections, the results are summarized for the electrical acceptance tests of the modules in their individual metal boxes (section 3.5).

#### *4.3.1. Module Leakage Currents*

Fig. 23 shows a sample of IV (module leakage current for the sum of the four sensors versus bias voltage) curves for 100 individual modules, measured at 15 °C, taken with voltage steps of 10 V and 10 s settling time at each voltage. It is seen that the large majority of modules have good behaviour up to 500 V bias, while a small number show a rise in current caused by strip micro-discharge above 350 V. In total, ~ 13% of all modules show the onset of strip micro-discharge between 350 V and 500 V.

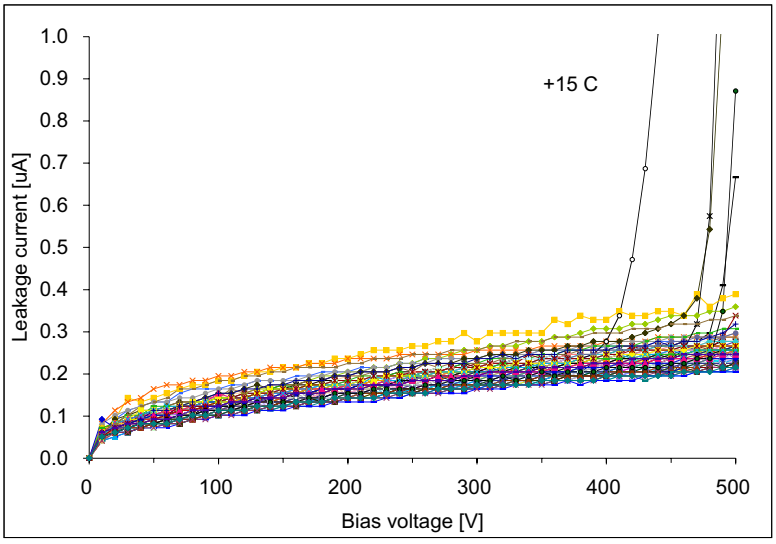



Fig. 23: IV characteristics measured at 15 °C for a sample of 100 barrel modules. Five modules show micro-discharge above 350 V bias.

In Fig. 24, the distributions of module leakage currents at 350 V bias and 500 V bias are shown, normalized to a temperature of 20 °C, for 2495 modules. The mean currents are very low; 503 nA at 350 V bias and 540 nA at 500 V bias. Modules showing micro-discharge above 350V are excluded from the 500V bias data.

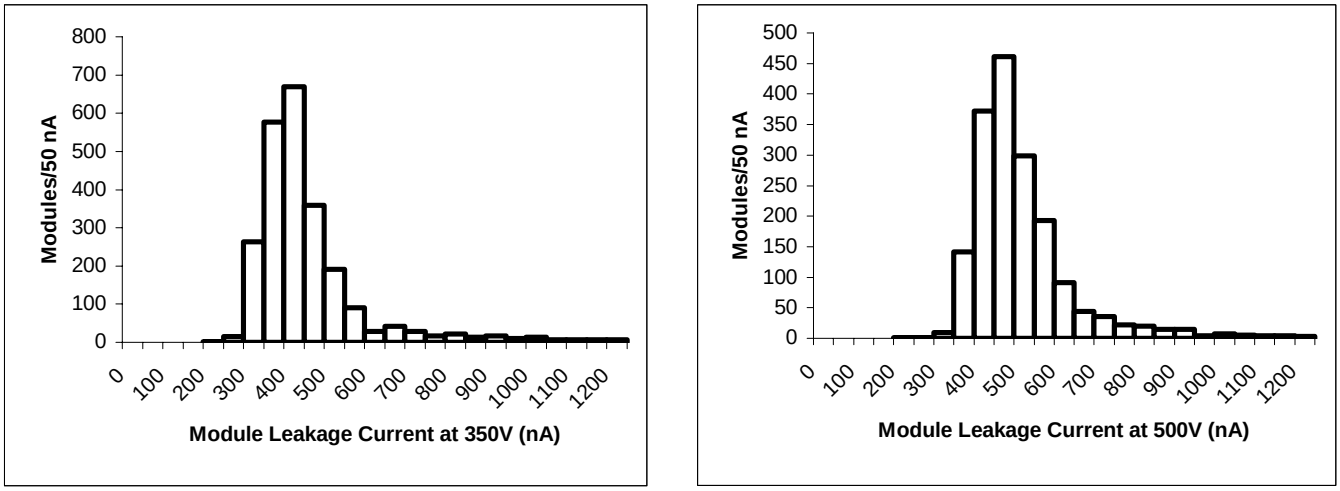



Fig. 24: Measured leakage currents of modules, normalized to 20°C: left at 350 V bias, right at 500 V bias.

*4.3.2. Module Noise, Gain and Offset*

As stated in section 3.5, the channel gain, discriminator offset and ENC at the discriminator input can be extracted from the module response curves, obtained from threshold scans.

The uniformity of the results for each channel of a module has been illustrated in [8]. In Fig. 25 the distributions of the average gain per module, and the average ENC are shown, with the modules operating warm (a hybrid thermistor temperature of ~ 28 °C). The average gain is 55 mV/fC, and the average ENC is 1615 electrons at this operating temperature.

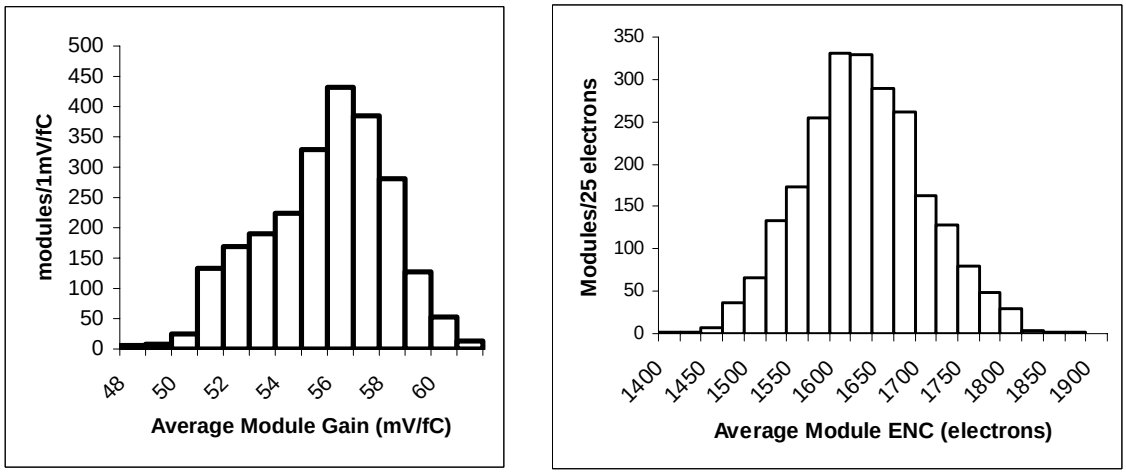



Fig. 25: Distributions of left: module gains, averaged over all channels in the module, and right: ENC, averaged over all channels in the module, at operational temperatures of ~28°C at the hybrid thermistors.

The ENC reduces with temperature by about 5 electrons per degree [8]. The average value at the operating temperature of ATLAS (~ 0 °C at the hybrid thermistor) is therefore ~ 1470 electrons. This corresponds to a signal:noise ratio of ~14:1, which is consistent with test beam measurements for the modules [33].

*4.3.3. Noise Occupancy*

In Fig. 26 the distribution of the mean noise occupancy per channel for all channels in the module at 1fC threshold is shown for the modules, operating warm (about 28 $^0$C at the hybrid thermistors). The average value, $4.5 \times 10^{-5}$, is an order of magnitude less than the specified maximum value.

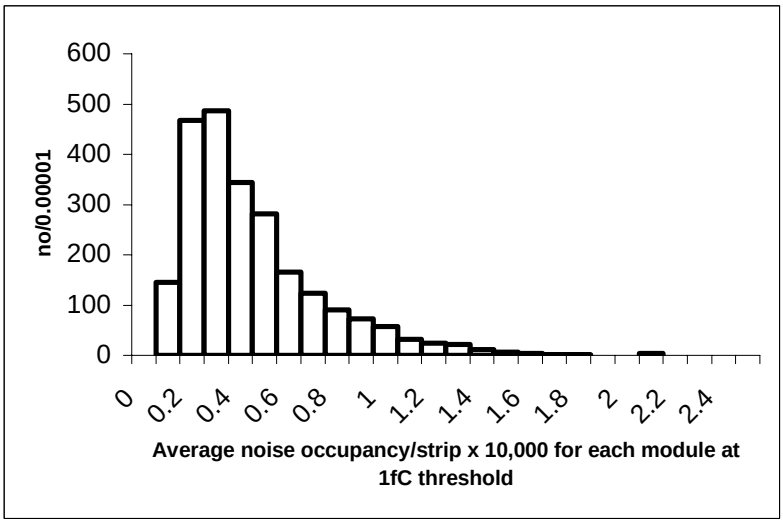



Fig. 26: Distribution of the average noise occupancy/channel at 1fC binary threshold for the modules, measured with a hybrid thermistor temperature of ~ 28 ºC.

### *4.3.4. Bad Readout Strips*

Fig. 27 shows the distribution of the number of bad readout strips per module, as defined in section 2.3.4. The average is 2.6 per module, that is, 99.8% of the module readout strips are good.

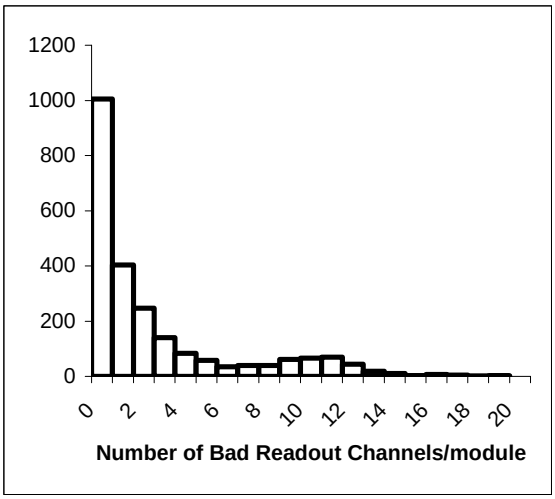



Fig. 27: Distribution of number of bad readout channels per module for the modules.

It is seen that there is a subsidiary peak in Fig. 27, centred around 11 bad channels in a module. This is caused by the use of some hybrids that were loaded with ASICs with 1 bad channel, as described in section 3.2.2. Bad channels in ASICs and localized damage to the silicon in wire-bonding are the dominant causes of bad channels in the modules. However, the achievement of 99.8% good readout channels overall is well above the 99% specification for the modules.

*4.4. Non-irradiated and Irradiated Module test-beam results*

The performance of barrel modules has been evaluated during their development and their series production in the H8 test-beam at CERN, and also in a KEK test-beam. At CERN, the beam is of high momentum (180 GeV pions), and the modules can be placed within a 1.56 T magnetic field, with the possibility of rotating the angle of the face of the silicon with respect to the incident tracks over the ± 20$^{o}$ range relevant to barrel modules within ATLAS.

Both irradiated and non-irradiated modules have been evaluated in the beam tests. The irradiation of the modules was uniform over their area and was carried out in the CERN PS to a fluence of $3x10^{14}$ /cm$^2$ 24 GeV/c protons (that expected after 10 years of operation in ATLAS), using the SCT irradiation facility [34,35]. The modules are all kept cold, with the hybrids operating at about 0 $^{o}$C, as anticipated in ATLAS. A beam telescope is used to define precise track positions at the module planes.

The procedures and results of the test-beam studies are fully described in [33]. The principal conclusions relating to the performance of the barrel modules are:

(a) The resolution per module side in a direction perpendicular to the strips has the expected value of (strip pitch)/√12, that is, 23 μm, for tracks of normal incidence. This provides a module precision of 17 μm in r-phi when using correlated hits from the sensors on the two sides.

(b) The silicon sensors digitize with full efficiency to the centres of the outermost readout strips. The dead region in the centre of the module between the two silicon sensors (section 2.3.1) is ~ 2060 μm, slightly less than the physical distance of 2090 μm between the ends of the $p^+$ implants on the adjacent sensors.

(c) The median signal:noise value is ~13:1 for the non-irradiated modules, and ~ 10:1 for the irradiated modules, at 150 V and 450 V bias respectively, for tracks at normal incidence. The lower value after irradiation is principally due to higher noise, but is also affected by charge trapping.

(d) Both irradiated and non-irradiated modules can be operated at above 99% efficiency and below $5x10^{-4}$ noise occupancy (the SCT specifications) at around 1fC binary threshold, as required, at bias voltages of 150 V for non-irradiated modules and 450 V for fully irradiated modules. The operating window in threshold is larger for the non-irradiated than for the irradiated modules, because of the higher noise post-irradiation.

The test-beam results therefore indicate that the barrel modules will operate satisfactorily, to specification, within ATLAS over the planned lifetime of the tracker.

## 5. Initial Results from the assembled SCT Barrels

The barrel modules are assembled to four carbon-fibre barrel structures within the SCT (Table 1). The mounting and initial testing of all the 2112 modules on Barrels 3, 4, 5 and 6 took place over the period from June 2004 to August 2005 [36]. The process is described in detail elsewhere [37,38,39,40]. The four completed barrels were shipped to CERN, where they have been assembled together, within a sealed thermal enclosure. The SCT four-barrel assembly was then mounted within the barrel TRT to form the first part of the Inner Tracking Detector, ready for insertion and commissioning within the ATLAS experiment.

Fig. 28 shows the modules mounted on the largest SCT barrel, Barrel 6. The 672 modules are arranged in 56 rows, each consisting of 12 modules. A close-up of the detail of the overlapping modules is shown in Fig. 11. Sixteen of the modules for each barrel had small retro-reflectors glued onto their upper beryllia facings in defined positions and orientations before these modules were mounted in prescribed positions on the barrel. These will form part of the geodetic network for the Frequency Scan Interferometry (FSI) real time alignment system under construction for the SCT [3].

The module mounting was successfully carried out using two essentially identical robots [40,41]. Only three modules (0.15%) were physically damaged in the process, while a further thirteen modules were replaced after their initial functionality tests on the barrel, mostly due to readout problems encountered with individual ASICs. All the mounted modules then satisfied the SCT specifications, and the high mounting yield allowed modules near the limits of the specification to be kept back as spares. The modules were assigned to the different barrels according to their electrical quality, with the best being on the inner barrels. These inner modules have to withstand the higher levels of irradiation in ATLAS, and they also individually subtend larger solid angles at the interaction point. The characteristic properties of modules mounted on each barrel are summarized in Table 16.

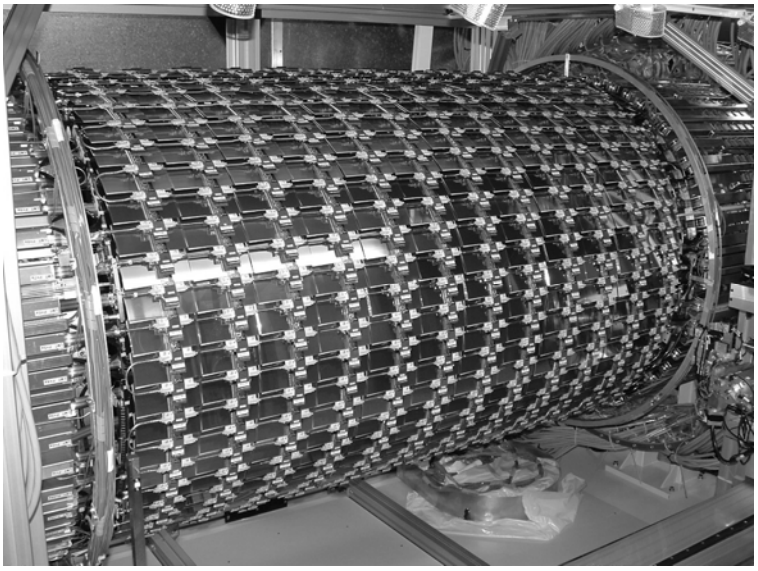
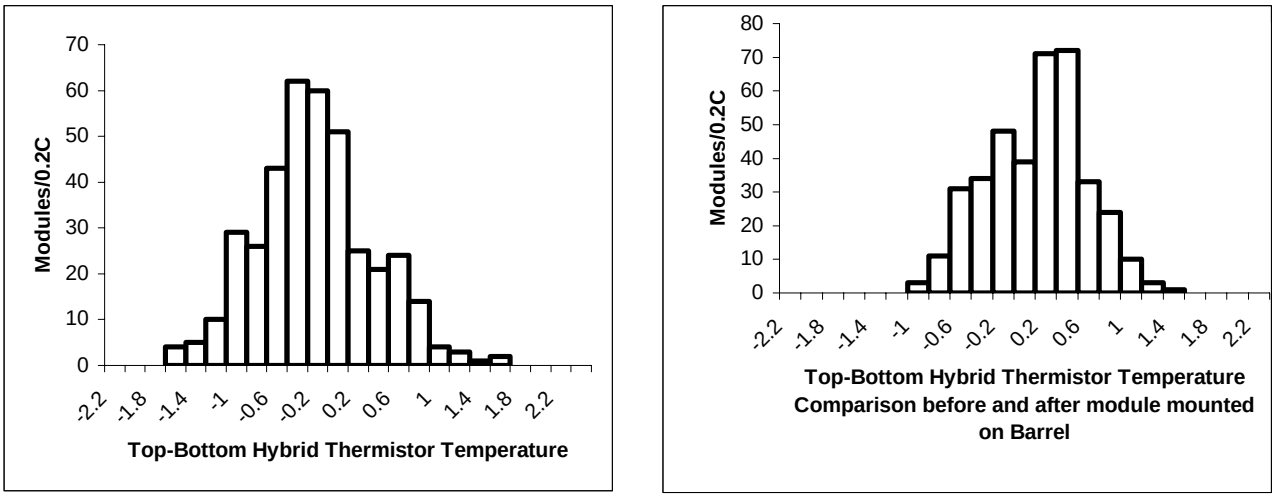


Fig. 28: Modules mounted on SCT Barrel 6, which is held within an assembly frame.

Table 16: The properties of modules mounted on each of the 4 SCT Barrels.

| | Barrel 3 | Barrel 4 | Barrel 5 | Barrel 6 |
|---|---|---|---|---|
| Minimum Bias Voltage for onset of sensor micro-discharge (section 2.3.4) | >500 V | >450 V | >400 V | >350 V |
| Inclusion of modules with ASICs having 1 bad analogue channel (section 3.1.3) | No | No | Yes (5% of Barrel 5) | Yes (28% of Barrel 6) |
| Temperature difference between thermistors on the 2 sides of the hybrid, when powered. | <2 $^{o}$C | <2 $^{o}$C | <2 $^{o}$C | <3 $^{o}$C |
| Angle of the cooling contact of the baseboard beryllia facing, b (Table 13) | <3 mrad | < 3 mrad | < 3 mrad | < 4 mrad |

On each separate barrel, following assembly, the modules have been powered simultaneously using final SCT low voltage and high voltage power supplies, and controlled and read out using final SCT readout electronics (Readout Drivers, Back of Crate optical interface cards, Timing module) [42,43,44]. Initial results are encouraging. All modules are fully functional and thermally well connected to their cooling blocks, via thermal grease [45]. The distribution of the mean hybrid thermistor temperature for each powered module is centred at 15 $^{o}$C above the temperature of the cooling pipe, which compares well with thermal FEA expectations (section 2.3.2), and the modules lie within ± 3 $^{o}$C of this value. The distribution of the difference in temperatures of the thermistors on the top and bottom faces of the module hybrid is shown in Fig. 29(a), for the 384 modules of Barrel 3, before being mounted on the barrel. In Fig. 29(b), the distribution of the change in this temperature difference is shown for each module before and after mounting on Barrel 3. The thermal integrity of all modules has been maintained, and hence also the mechanical integrity of the hybrid attachment, with all temperature differences still being less than 2 $^{o}$C for this barrel.




(a) (b)

Fig. 29: (a) The difference in temperatures, dT, of the thermistors on the top and bottom faces of the module hybrid for modules operated before being mounted on Barrel 3 and (b) the change in recorded dT for these modules when being operated before and after mounting on Barrel 3.

The gain, offset and noise have been measured for all modules on the barrels from threshold scans, and the noise occupancy. Data have been taken with the modules operated in small groups, and also with all modules operated together, with synchronized triggering [38]. There is no evidence for performance degradation (coming, for example, from coherent effects) in the large system. Also, the performance of a module on a barrel is very similar to that measured on the bench in its individual module box before mounting. This is illustrated in Fig. 30, where the distribution of the difference between the noise measured on the barrel and in the module box is shown for all mounted modules, both measurements being made at a similar hybrid thermistor temperature of ~ 28 $^{o}$C. The average ENC on the barrel is slightly lower, by just 16 electrons, and never more than 130 electrons higher than that measured in the box. Of the total of 3,244,032 readout channels on the SCT barrels, 99.8% are good. All modules on the barrels can be operated at the maximum specified bias voltage (Table 16) for the barrel, with similar room temperature leakage currents as before mounting. Thus the first tests of individually assembled SCT barrels have shown that they meet the performance specifications and requirements for ATLAS physics. The performance of the whole system will be measured when it operates within the barrel ATLAS TRT, and described in future publications.

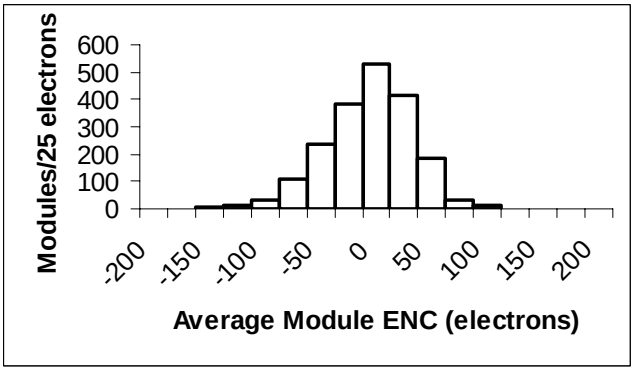



Fig. 30: The distribution of the difference in ENC, (barrel minus test box), measured at a hybrid thermistor temperature of ~ 28 $^{o}$C, for all the modules mounted on the four SCT barrels.

## 6. Summary

The R&D, prototyping and construction phases have been successfully completed for the barrel module project of the ATLAS SemiConductor Tracker. A total of 2582 modules have been constructed in four different SCT cluster locations during a two-year period of series production. The overall yield of modules with satisfactory mechanical and electrical performance is 90.5%. The required 2112 modules, to full ATLAS electrical and mechanical specification, have been mounted on the four barrel structures of the SCT. Module performance on the individual barrels, measured immediately after assembly, shows no degradation, with 99.8% good channels in the readout, low leakage currents and the predicted thermal performance.

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